

PRODUCT SPECIFICATION

PART NUMBER REV: FLC-156MML5000SA2

DESCRIPTION: TFT 15.6''W 1920*1080 Full View LVDS 1000CD + Led Cable

() Preliminary Specification

(V) Approved Specification

| | |
|-----------------------|--------------|
| Customer Name: | |
| Signature: | Date: |
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| | |
| PREPARED BY | REVIEWED BY |
| <i>Sarah Chen</i> | <i>David</i> |

Revision History

| Spec Version | Date | Page | Description | Note |
|--------------|------------|--------|---|------|
| V1.0 | 2019/9/23 | | First Edition | |
| V2.0 | 2019/10/03 | | Update Edition | |
| V3.0 | 2019/10/28 | P16 | Modify BLOCK DIAGRAM | |
| V4.0 | 2020/08/24 | P20 | The length of cable change | |
| V4.1 | 2020/03/03 | | Update Backlight, connector/Heatsink | |
| V4.2 | 2022/01/20 | P4.P21 | Update Dimension(D) and Drawing | |
| V4.3 | 2023/01/04 | P5 | Update Environment Absolute Rating note (3) | |
| | | | | |
| | | | | |

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1. GENERAL DESCRIPTION

1.1 Description

15.6" is a Color Active Matrix Liquid Crystal Display Module composed of a TFT LCD panel and LED backlight system. The screen format is intended to support the FHD, 1920x1080 screen and 16.2M colors.

1.2 Product Summary

The following items are summary on the table under Ta=25 °C condition:

| No. | Item | Specification | Unit |
|-----|--------------------------------|---|-------------------|
| 1 | Display Size | 15.6w | Inch |
| 2 | Pixel Number | 1920 (H) x 3(RGB)x 1080 (V) | Pixels |
| 3 | Outline Dimension | 363.8(W)×215.9(H)×9.3(D, max) | mm |
| 4 | Active Area | 344.16(H) X 193.59(V) | mm |
| 5 | Display Colors | 16.2M | -- |
| 6 | Pixel Arrangement | RGB vertical stripe | -- |
| 7 | Display Mode | Full View / Normally Black | -- |
| 8 | Electrical Interface | LVDS | -- |
| 9 | Surface Treatment | Anti-Glare, 3H hard coating | -- |
| 10 | Brightness | 1000 (Typ.) | cd/m ² |
| 11 | Contrast Ratio | 800 (Typ.) | -- |
| 12 | Total Power Consumption (Typ.) | 16 W (VDD line=4 W; LED lines= 12 W) | W |

2. ABSOLUTE MAXIMUM RATING

2.1 Electrical Absolute Rating

| Item | Symbol | Values | | | Unit | Note |
|----------------------|--------|--------|-----|-----|------|------------------|
| | | Min | Typ | Max | | |
| Power supply voltage | Vcc | -0.3 | - | 3.6 | V | (1) |
| Logic Input Voltage | VIN | -0.3 | - | 4.0 | V | |
| LED Current | I LED | -- | 600 | -- | mA | Duty=100% (1)(2) |

Note (1) Permanent damage to the device may occur if max values are exceeded.

Function operation should be restricted to the conditions described under normal operating conditions.

(2) Specified values are for input pin of LED light bar at $T_a=25\pm 2^{\circ}\text{C}$

2.2 Environment Absolute Rating

| Item | Symbol | Values | | | Unit | Note |
|-----------------------|--------|--------|-----|------|------|------------|
| | | Min | Typ | Max. | | |
| Operating Temperature | Top | -30 | | 85 | °C | |
| Storage Temperature | Tstg | -40 | | 90 | °C | Note(1)(2) |

Note (1) Max O.T. LCD surface Temperature

Note (2) Permanent damage to the device may occur if exceed maximum values

Note (3) In the standard conditions, there is no function failure issue occurred. All the cosmetic specification is judged before reliability test.

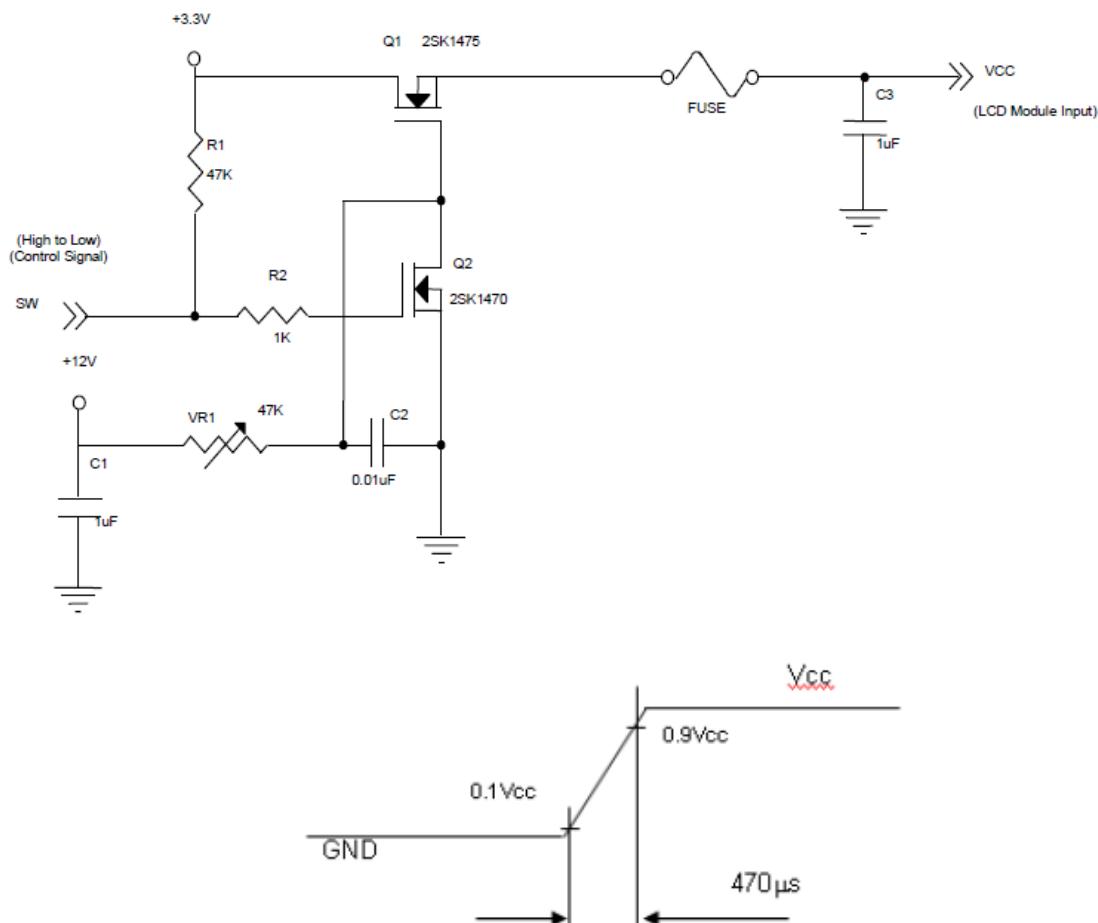
3. ELECTRICAL CHARACTERISTICS

3.1 LCM

| Parameter | Symbol | Value | | | Unit | Note |
|---------------------------------|-------------------|-------|------|------|------|------|
| | | Min. | Typ. | Max. | | |
| Power Supply Voltage | VCC | 3.0 | 3.3 | 3.6 | V | |
| Ripple Voltage | VRP | -- | -- | 150 | mV | |
| Rush Current | I _{RUSH} | -- | -- | 3.0 | A | (2) |
| Power Supply Current | White | -- | 1.22 | 1.5 | A | (3) |
| | Black | -- | 0.51 | 0.7 | A | |
| | Vertical Stripe | -- | 0.82 | 1 | A | |
| Power Consumption | PLC | -- | 4 | 5 | W | |
| LVDS differential input voltage | V _{id} | 200 | -- | 600 | mV | (4) |
| LVDS common input voltage | V _{ic} | 1.0 | 1.2 | 1.4 | V | (4) |
| Terminating Resistor | R _T | | 100 | | Ohm | |

Note (1) The assembly should be always operated within above ranges. $T_a = 25 \pm 2 {}^\circ C$

Note (2) Measurement Conditions:

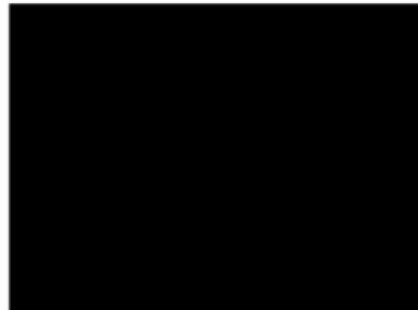


Note (3) The specified power supply current is under the conditions at Vcc=3.3V, Fr=60Hz, whereas a power dissipation check pattern below is displayed

a. White Pattern

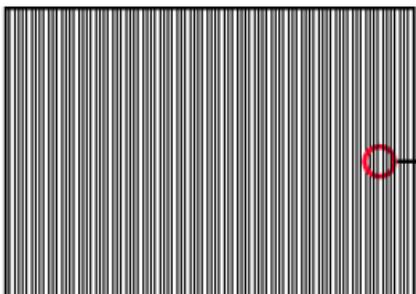


b. Black Pattern



Active Area

c. Vertical Stripe Pattern



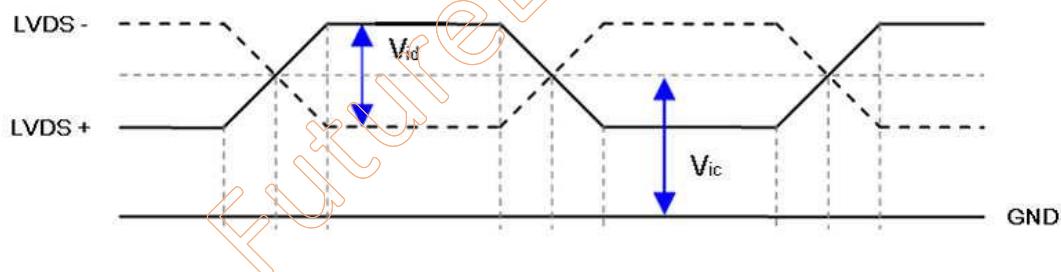
Active Area



Active Area

Note (4) The power consumption is specified at the pattern with the maximum current.

Note (5) VID waveform condition.



3.2 Backlight Unit

Parameter guideline for LED driving is under stable conditions at 25°C (Room Temperature):

| Parameter | Min. | Typ. | Max. | Unit | Note |
|--------------------------|------|---------|------|------|---------|
| LED voltage (VL) | | 39 | | | V |
| LED current (IL-channel) | | 300 | | | mA |
| LED Power (PL) | | 11,7 | | | W |
| LED life Time (Typical) | -- | 100,000 | -- | Hrs | (2) (1) |

Note 1: The “LED lift time” is defined as the module brightness decrease to 50% original brightness that the ambient temperature is 25°C and typical LED Current at 300 mA/channel.

Note 2: PL=VL x IL

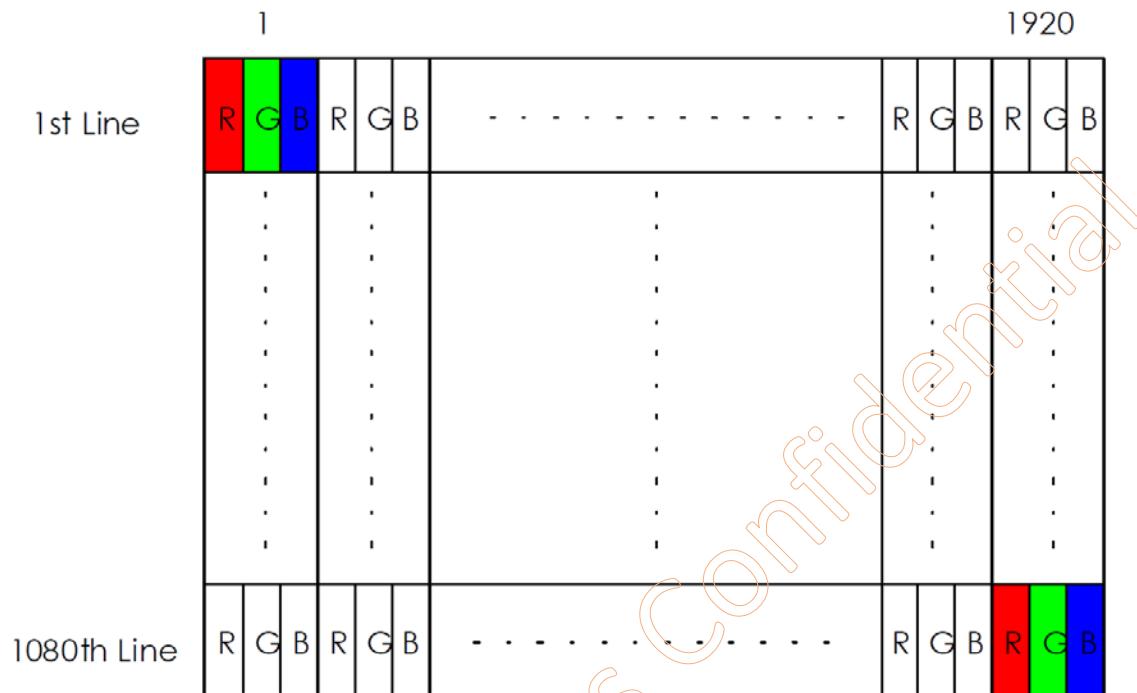
LED Bar Connector: JOIN TEK JT1025-1021 (BHSR-02VS-1)

| Pin no | Symbol | I/O | Description | Remark |
|--------|--------|-----|-----------------------|--------|
| 1 | VLED+ | P | Backlight LED anode | Red |
| 2 | VLED- | P | Backlight LED cathode | Black |

3.3 Signal Interface Characteristic

1. Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



2. Scanning Direction

The following figures show the image seen from the front view. The arrow indicates the direction of scan.

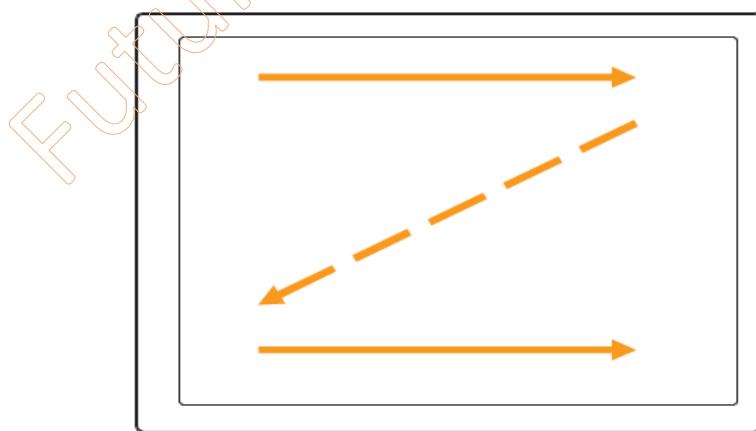


Fig. 1 Normal scan (Pin4, DPS = Low or NC)

4. SIGNAL CHARACTERISTICS

4.1 Interface Timing

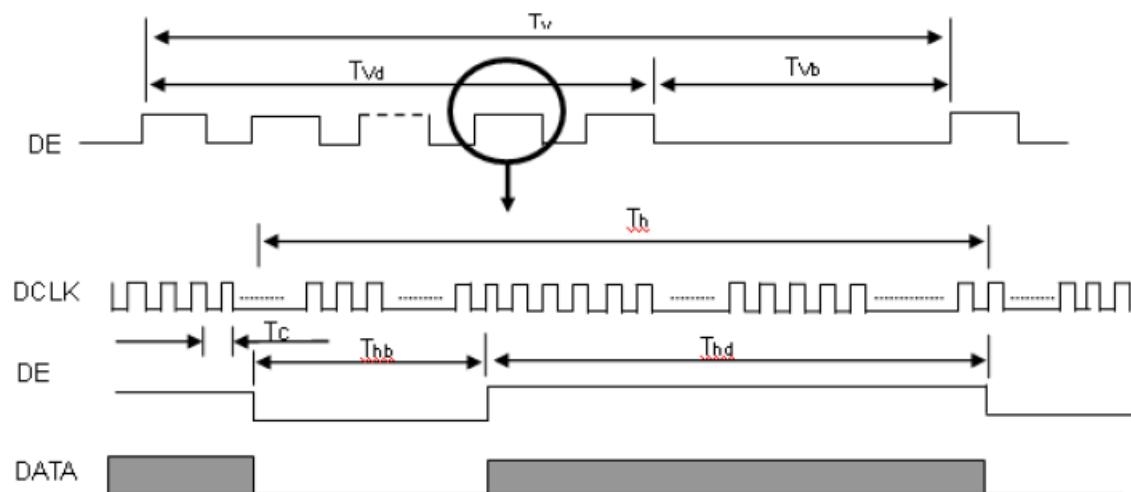
4.1.1 Timing Characteristics:

| Signal | Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|-------------------------|--------------------------------------|------------------------|---------------------------------|-------|---------------------------------|----------------|--|
| LVDS Clock | Frequency | F _c | 60 | 70.93 | 75 | MHZ | |
| | Period | T _c | -- | 14.1 | -- | ns | |
| | Input cycle to cycle jitter | T _{rd} | -0.02*T _c | -- | 0.02*T _c | ns | (3) |
| | Input Clock to data skew | T _{LVCCS} | -0.02*T _c | -- | 0.02*T _c | ps | (4) |
| | Spread spectrum modulation range | F _{clkin_mod} | F _c *98% | -- | F _c *102% | MHz | (5) |
| | Spread spectrum modulation frequency | F _{SSM} | -- | -- | 200 | KHz | |
| Vertical Display Term | Frame Rate | F _r | 50 | 60 | 60 | Hz | T _v =T _{vD} +T _{vB} |
| | Total | T _v | 1090 | 1110 | 1130 | Th | -- |
| | Display | T _{vD} | 1080 | 1080 | 1080 | Th | -- |
| | Blank | T _{vB} | T _v -T _{vD} | 30 | T _v -T _{vD} | Th | -- |
| Horizontal Display Term | Total | T _h | 1050 | 1065 | 1075 | T _c | T _h =T _{hd} +T _{hb} |
| | Display | T _{hd} | 960 | 960 | 960 | T _c | -- |
| | Blank | T _{hb} | T _h -T _{hd} | 105 | T _h -T _{hd} | T _c | -- |

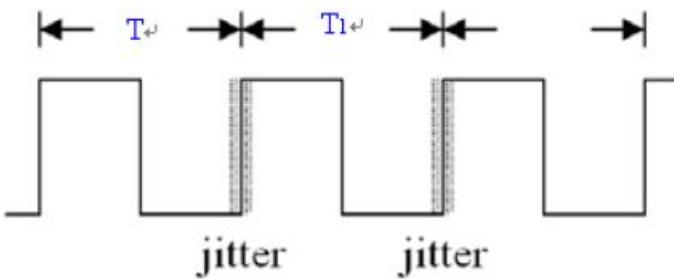
Note (1) Because this module is operated by DE only mode. Hsync and Vsync input signals are ignored.

Note (2) The T_v(T_{vD}+T_{vB}) must be integer, otherwise, this module would operate abnormally.

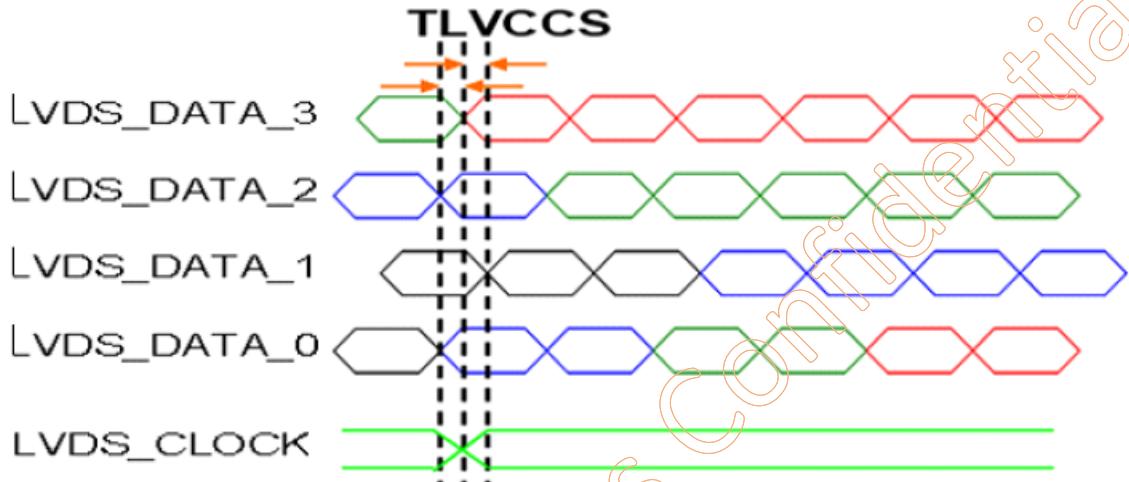
INPUT SIGNAL TIMING DIAGRAM



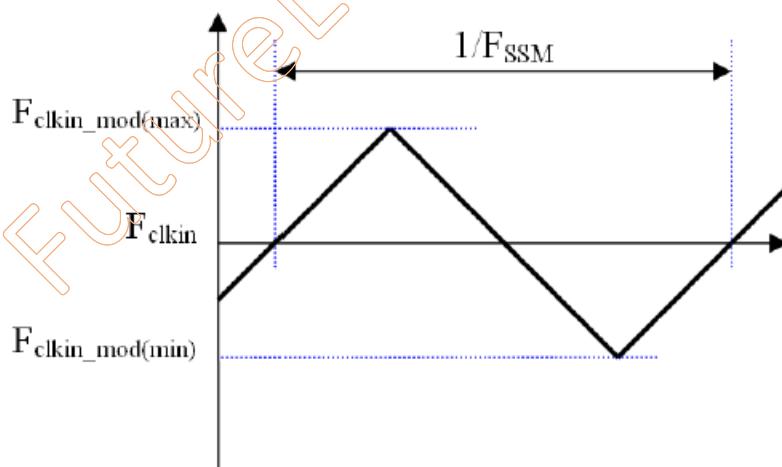
Note (3) The input clock cycle-to-cycle jitter is defined as below figures. $T_{rcl} = |T_1 - T|$



Note (4) Input Clock to data skew is defined as below figures.

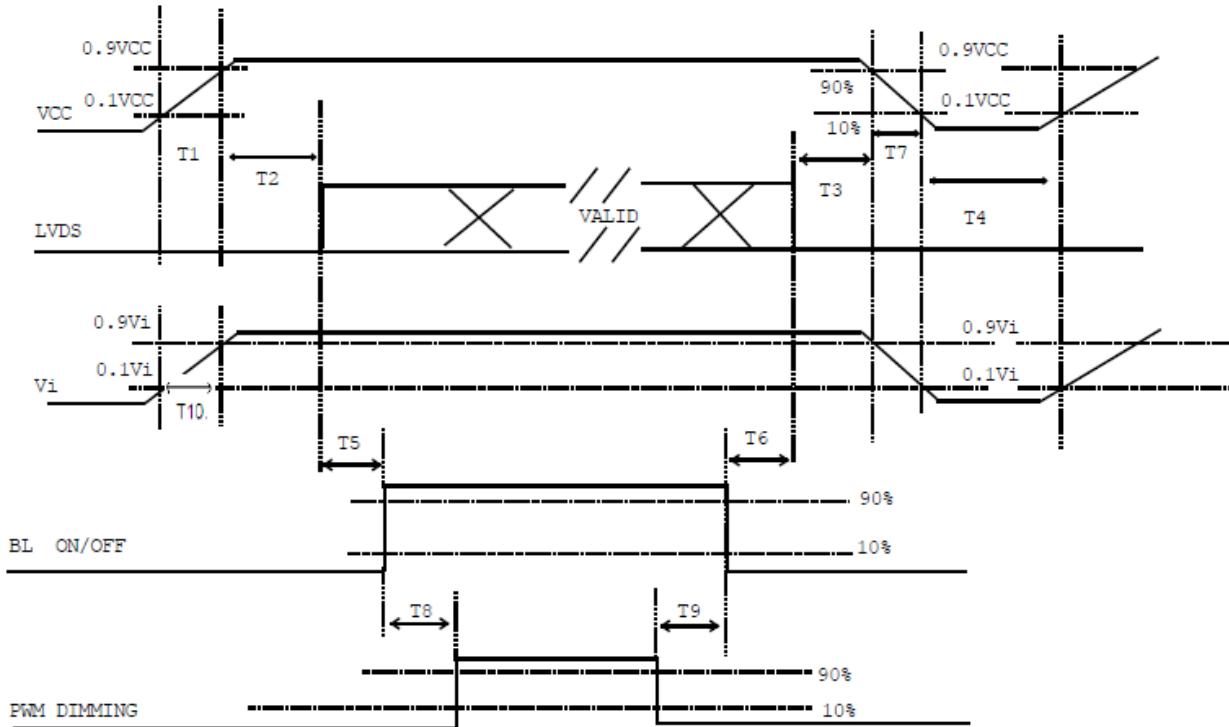


Note (5) The SSCG (Spread spectrum clock generator) is defined as below figures.



4.1.2 Power ON/OFF Sequence

To prevent a latch-up or DC operation of LCD assembly, the power on/off sequence should be as the diagram below.



Timing specifications:

| Parameter | Value | | | Units |
|-----------|-------|-----|-----|-------|
| | Min | Typ | Max | |
| T1 | 0.5 | - | 10 | ms |
| T2 | 0 | - | 50 | ms |
| T3 | 0 | - | 50 | ms |
| T4 | 500 | - | | ms |
| T5 | 450 | - | | ms |
| T6 | 20 | - | | ms |
| T7 | 10 | - | 300 | ms |
| T8 | 10 | - | | ms |
| T9 | 10 | - | | ms |
| T10 | 20 | - | | ms |

Note (1) Please avoid floating state of interface signal at invalid period.

Note (2) When the interface signal is invalid, be sure to pull down the power supply of LCD VCC to 0V.

Note (3) The Backlight converter power must be turned on after the power supply for the logic and the interface

signal is valid.

The Backlight converter power must be turned off before the power supply for the logic and the interface signal is invalid.

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5. INTERFACE PIN DESCRIPTION

5.1 LCM Connector PIN Assignment

| NO | Symbol | Description | Note |
|----|----------|---|----------|
| 1 | NC | Not connection, this pin should be open | - |
| 2 | NC | Not connection, this pin should be open | - |
| 3 | NC | Not connection, this pin should be open | - |
| 4 | NC | Not connection, this pin should be open | - |
| 5 | GND | Ground | - |
| 6 | GND | Ground | - |
| 7 | GND | Ground | |
| 8 | GND | Ground | |
| 9 | NC | Not connection, this pin should be open | - |
| 10 | NC | Not connection, this pin should be open | - |
| 11 | LCD_Vcc | LCD logic and driver power 3.3V | |
| 12 | LCD_Vcc | LCD logic and driver power 3.3V | |
| 13 | LCD_Vcc | LCD logic and driver power 3.3V | |
| 14 | NC | No connection | - |
| 15 | NC | No connection | - |
| 16 | NC | No connection | - |
| 17 | REV SCAN | Low or NC- Normal Mode. High- Horizontal & Vertical Reverse Scan | Note (3) |
| 18 | RXO0- | Negative LVDS differential data input. CHO0(odd) | - |
| 19 | RXO0+ | Positive LVDS differential data input. CHO0(odd) | - |
| 20 | RXO1- | Negative LVDS differential data input. CHO1(odd) | |
| 21 | RXO1+ | Positive LVDS differential data input. CHO1(odd) | |
| 22 | RXO2- | Negative LVDS differential data input. CHO2(odd) | |
| 23 | RXO2+ | Positive LVDS differential data input. CHO2(odd) | |
| 24 | LCD GND | LCD logic and driver ground | |

| | | | |
|----|---------|--|--|
| 25 | RXOC- | Negative LVDS differential clock input (odd) | |
| 26 | RXOC+ | Positive LVDS differential clock input (odd) | |
| 27 | LCD GND | LCD logic and driver ground | |
| 28 | RXO3- | Negative LVDS differential data input. CHO3(odd) | |
| 29 | RXO3+ | Positive LVDS differential data input. CHO3(odd) | |
| 30 | RXE0- | Negative LVDS differential data input. CHE0 (even) | |
| 31 | RXE0+ | Positive LVDS differential data input. CHE0 (even) | |
| 32 | RXE1- | Negative LVDS differential data input. CHE1 (even) | |
| 33 | RXE1+ | Positive LVDS differential data input. CHE1 (even) | |
| 34 | LCD GND | LCD logic and driver ground | |
| 35 | RXE2- | Negative LVDS differential data input. CHE2 (even) | |
| 36 | RXE2+ | Positive LVDS differential data input. CHE2 (even) | |
| 37 | RXEC- | Negative LVDS differential clock input (even) | |
| 38 | RXEC+ | Positive LVDS differential clock input (even) | |
| 39 | RXE3- | Negative LVDS differential data input. CHE3 (even) | |
| 40 | RXE3+ | Positive LVDS differential data input. CHE3 (even) | |

Note (1) Connector Part no.: I-PEX 20455-040E-76 or equivalent.

Note (2) User's connector Part no. I-PEX 20453-040T-03 or equivalent.

Note (3) "Low" stands for 0V. "High" stands for 3.3V. "NC" stands for "No Connected".

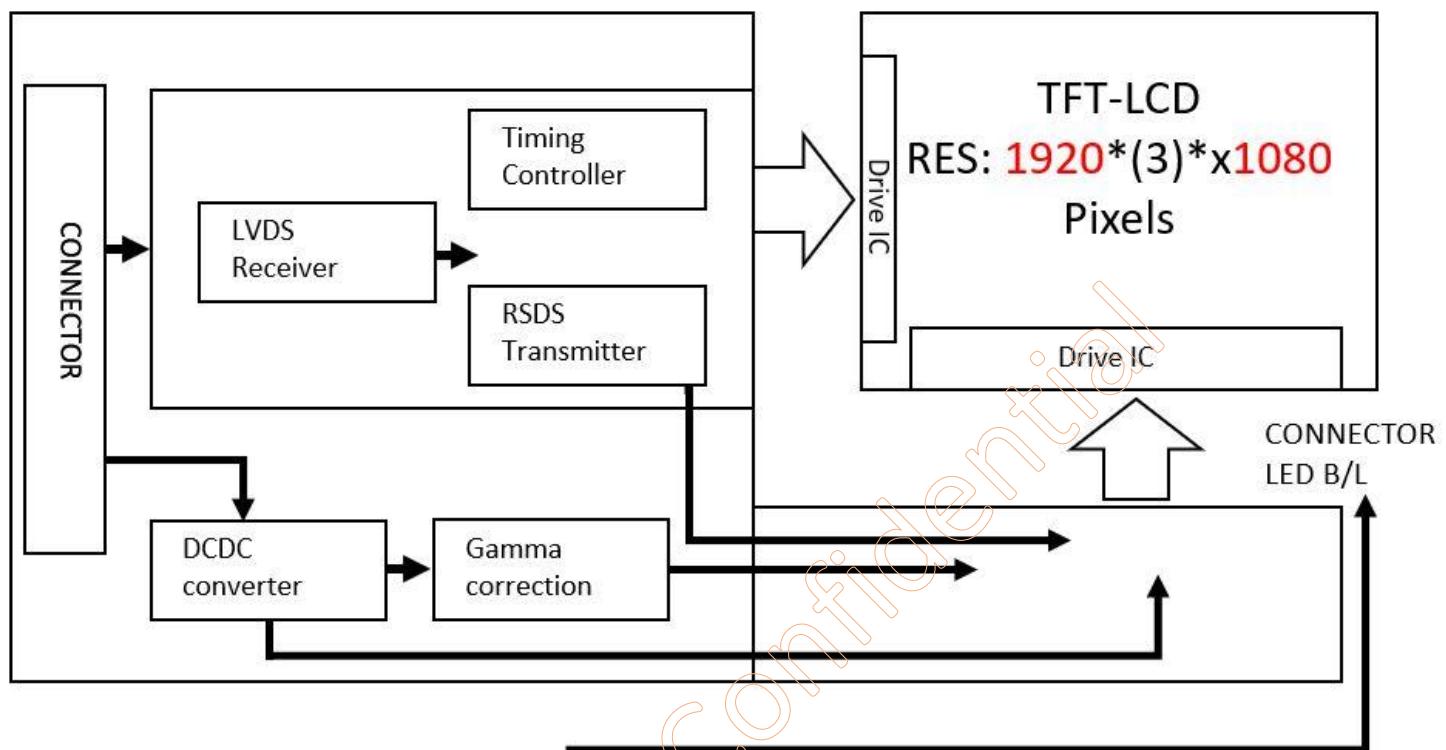
5.2 LVDS DATA MAPPING TABLE

| | | | | | | | | |
|-----------------|-------------|-----|-----|-----|-----|-----|-----|-----|
| LVDS Channel O0 | LVDS output | D7 | D6 | D4 | D3 | D2 | D1 | D0 |
| | Data order | OG0 | OR5 | OR4 | OR3 | OR2 | OR1 | OR0 |
| LVDS Channel O1 | LVDS output | D18 | D15 | D14 | D13 | D12 | D9 | D8 |
| | Data order | OB1 | OB0 | OG5 | OG4 | OG3 | OG2 | OG1 |
| LVDS Channel O2 | LVDS output | D26 | D25 | D24 | D22 | D21 | D20 | D19 |
| | Data order | DE | NA | NA | OB5 | OB4 | OB3 | OB2 |
| LVDS Channel O3 | LVDS output | D23 | D17 | D16 | D11 | D10 | D5 | D27 |
| | Data order | NA | OB7 | OB6 | OG7 | OG6 | OR7 | OR6 |
| LVDS Channel E0 | LVDS output | D7 | D6 | D4 | D3 | D2 | D1 | D0 |
| | Data order | EG0 | ER5 | ER4 | ER3 | ER2 | ER1 | ER0 |
| LVDS Channel E1 | LVDS output | D18 | D15 | D14 | D13 | D12 | D9 | D8 |
| | Data order | EB1 | EB0 | EG5 | EG4 | EG3 | EG2 | EG1 |
| LVDS Channel E2 | LVDS output | D26 | D25 | D24 | D22 | D21 | D20 | D19 |
| | Data order | DE | NA | NA | EB5 | EB4 | EB3 | EB2 |
| LVDS Channel E3 | LVDS output | D23 | D17 | D16 | D11 | D10 | D5 | D27 |
| | Data order | NA | EB7 | EB6 | EG7 | EG6 | ER7 | ER6 |

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6. BLOCK DIAGRAM

The following diagram shows the functional block of the TFT module:



7. OPTICAL CHARACTERISTIC

The optical characteristics are measured under stable conditions at room temperature.

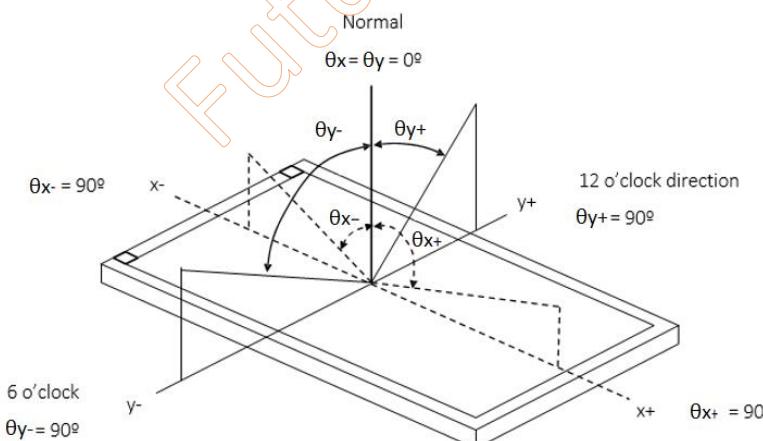
| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Note | | |
|---------------------------|------------|---|-------|-------|------|-------------------|--------|---|--|
| Contrast Ratio | CR | $\theta_X=0^\circ, \theta_Y = 0^\circ$ Viewing angle at normal direction | 600 | 800 | - | - | (2)(5) | | |
| Response Time | TR | | - | 13 | - | ms | (3) | | |
| | TF | | - | 12 | - | ms | | | |
| Center Luminance of White | LC | | 800 | 1000 | - | cd/m ² | (4)(5) | | |
| White Variation | δW | | 70 | 75 | -- | % | (5)(6) | | |
| Chromaticity | Red | | Typ. | 0.652 | Typ. | - | (1) | | |
| | | | | 0.338 | | - | | | |
| | Green | | | 0.333 | | - | | | |
| | | | | 0.613 | | - | | | |
| | Blue | | | 0.150 | | - | (5) | | |
| | -0.05 | | 0.050 | +0.05 | - | | | | |
| | | | White | | | 0.313 | | - | |
| | | | | | | 0.329 | | - | |
| Viewing Angle | Horizontal | $CR \geq 10$ | 80 | 85 | - | Deg. | (1)(5) | | |
| | | | 80 | 85 | - | | | | |
| | Vertical | | 80 | 85 | - | | | | |
| | | | 80 | 85 | - | | | | |

The following optical specifications shall be measured in a darkroom or equivalent state (ambient luminance <2 lux, and at room temperature).

The room temperature is $25^{\circ}\text{C} \pm 2^{\circ}\text{C}$.

Note 1: Definition of Viewing Angle

Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or the vertical clock direction with respect to the optical axis which is normal to the LCD surface

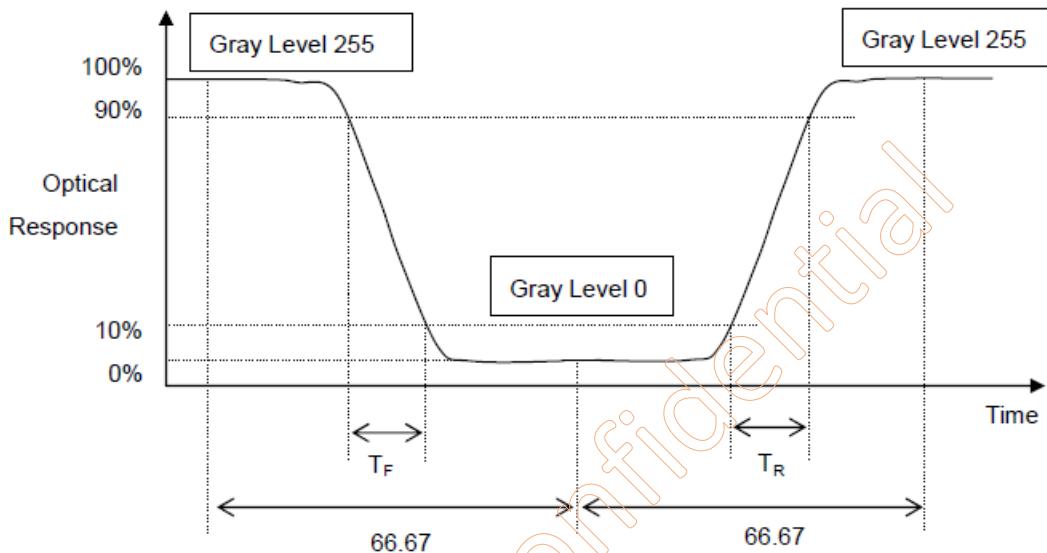


Note 2: Definition of Contrast Ratio (CR)

Measure the viewing angle of $\Theta=0$ and at the center of the LCD surface. Luminance with all pixels in white state divide by Luminance with all pixels in Black state

Note 3 Definition of Response Time:

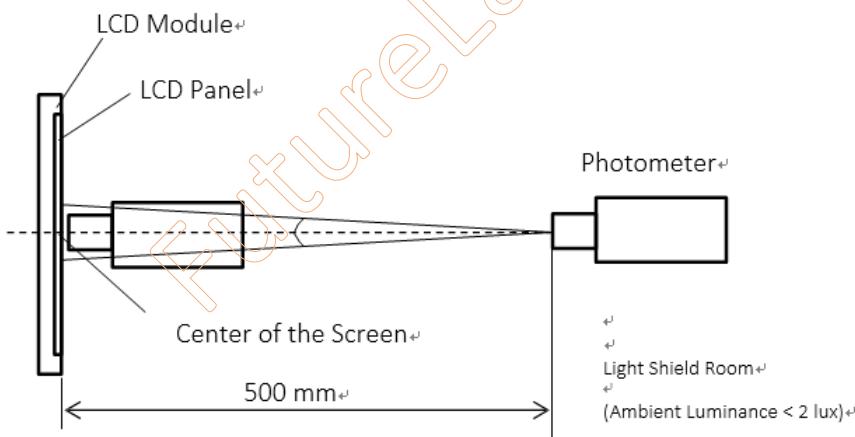
The response time is set initially by defining the “Rising Time (T_R)” and the “Falling Time (T_F)” respectively. Please refer the figure to the followings:



Note 4: Definition of Brightness (L)

Measure the center area of the panel and the viewing angle of the $\theta_x=\theta_y=0^\circ$

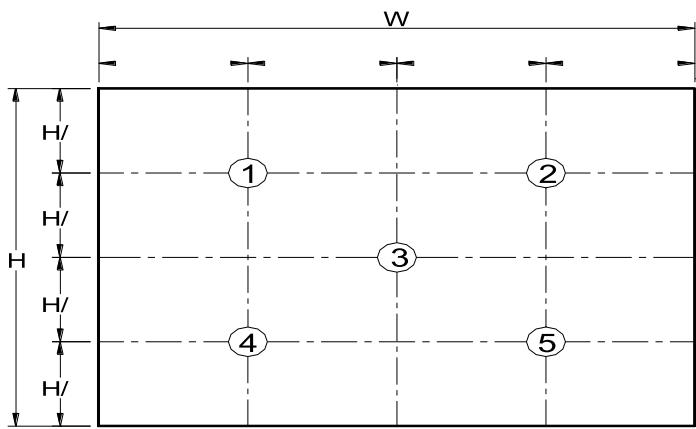
Note 5: The method of optical measurement:



Note 6: Definition of White Variation (δW):

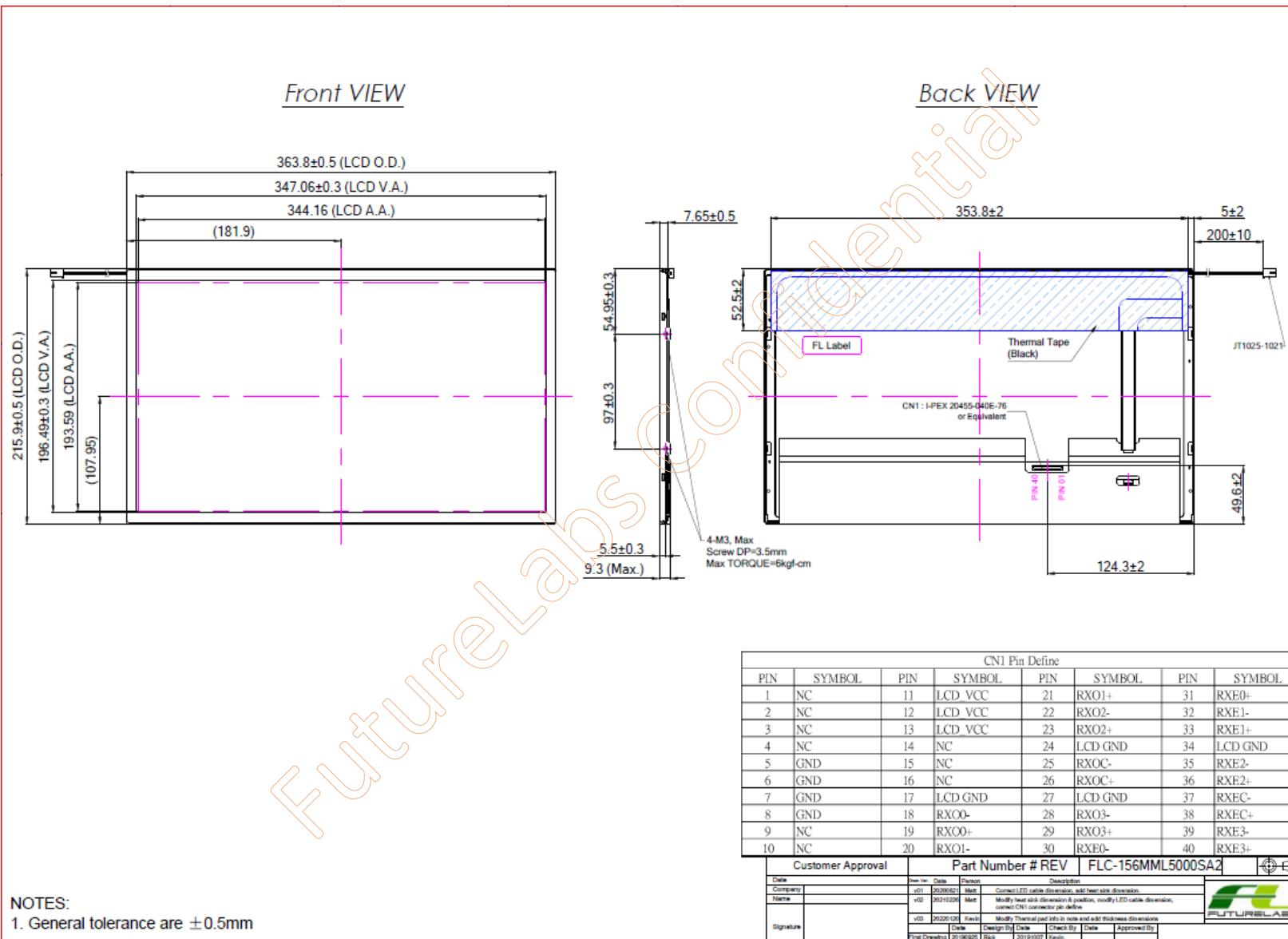
Measure the luminance of gray level 255 at 5 points

$$\delta W = \{ \text{Maximum} [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum} [L(1), L(2), L(3), L(4), L(5)] \} * 100\%$$



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8. DIMENSION AND DRAWING



NOTES:

1. General tolerance are $\pm 0.5\text{mm}$

9. PRECAUTION AND PRODUCT HANDLING

- Do not apply the external force such as bending or twisting to the LCD panel and backlight during assembly.
- Do not insert and plug out the input connector while the LCD panel is operating.
- Do not take apart the panel or frame from LCD module assembly or insert anything into the backlight unit.
- Do not keep the same pattern in a long period of time, it may cause image sticking on LCD panel. Can use shuffle content periodically if fixed pattern is displayed on the screen.
- Do not touch the display area with bare hands, this will stain the display area.
- Pay attention to handle lead wire of backlight, that is not tugged in connect with LED driver.
- Do not change variable resistance settings in LCD panel, it may cause not satisfy of LCD characteristics specification.
- The surface of LCD panel's polarizer is very soft and easily scratched, please use a very soft dry cloth without chemicals for cleaning.
- To avoid the static electricity to damage the CMOS LSI, the operator should be grounded when in contact with the LCD panel, and also to all electrical equipment.
- Need to follow the correct power frequency when LCD panel is connecting and operating, this can avoid damage to CMOS LSI during latch-up.
- Need to store the LCD panel indoor without the exposure of sunlight where the temperature is $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ and the humidity is below 60% RH.