

PRODUCT SPECIFICATION

PART NUMBER: QX-101WSVGATLT00S
DESCRIPTION: TFT 10.1"wide 1024*600 TN LVDS 400CD

Rev:4.0

- () Preliminary Specification
- (V) Approved Specification

Customer Name:	
Signature:	Date:

QiteX Advanced Display Solution		
PREPARED BY	REVIEWED BY	SIGNATURE DATE
<i>Natalie Lin</i>	<i>Joy Tseng</i>	<i>2019/06/19</i>

1. Precautions and Warranty

1.1 Precaution

- 1.1.1 Do not apply rough force such as bending or twisting to the module during assembly.
- 1.1.2 To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- 1.1.3 Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- 1.1.4 It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.
- 1.1.5 Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- 1.1.6 Do not pull the I/F connector in or out while the module is operating.
- 1.1.7 Do not disassemble the module, or insert anything into the Backlight unit
- 1.1.8 It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.
- 1.1.9 High temperature or humidity may reduce the performance of module. Please store LCD module
- 1.1.10 within the specified storage conditions.
- 1.1.11 The response time will become slowly below lower temperature.
- 1.1.12 Do not keep same pattern in a long period of time. It may cause image sticking on LCD.
- 1.1.13 Display may change color with different temperature.
- 1.1.14 The Module should be kept into anti-static bag or other containers resistant to static for storage.
- 1.1.15 If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- 1.1.16 After the module's end of life, it is not harmful in case of normal operation and storage.

1.2 Warranty

- 1.2.1 Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss.
- 1.2.2 If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.

2. GENERAL DESCRIPTION

The specification is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This product is composed of a TFT-LCD panel, driver ICs and a backlight unit.

2.1 General Specifications

Features	Details	Unit
Display Size(Diagonal)	10.1"	
LCD type	TN TFT	
Display Mode	Transmissive/ Normally White	
Resolution	1024 RGB x 600	Pixels
View Direction	12 O'CLOCK	Best Image
Gray Scale Inversion Direction	6 O'CLOCK	
Module Outline	235(H) x 143(V) x2.8(T) (Note1)	mm
Active Area	222.72(H) x125.28(V)	mm
Pixel Size	0.2175(H) x 0.2088(V)	mm
Pixel Arrangement	RGB Vertical Stripe	
Polarizer Surface Treatment	Anti-glare	
Display Colors	262K/16.7M	
Interface	6/8 bits-LVDS interface	
With or Without Touch Panel	Without	
Operating Temperature	-20~70	°C
Storage Temperature	-30~80	°C
Weight	TBD	g

Note: Exclusive posts, FFC/FPC tail etc.

3. Absolute Maximum Ratings

3.1 Absolute Ratings of Environment

$V_{SS}=0V, T_a=25^{\circ}C$

Item	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	-0.5	+3.96	V
	AVDD	-0.5	+14.85	V
	VGH	-0.3	+42.0	V
	VGL	VGH-42	+0.3	V
Storage temperature	T_{stg}	-30	+80	$^{\circ}C$
Operating temperature	T_{op}	-20	+70	$^{\circ}C$

Note 1: If T_a below $50^{\circ}C$, the maximal humidity is 90%RH, if T_a over $50^{\circ}C$, absolute humidity should be less than 60%RH.

Note 2: The response time will be extremely slow when the operating temperature is around $-10^{\circ}C$, and the back ground will become darker at high temperature operating.

3.2 Electrical Absolute Ratings

3.2.1 TFT LCD Module

Item	Symbol	Min.	Typ.	Max.	Unit	
Supply Voltage	VDD	3.0	-	3.6	V	
	AVDD	6.5	10.8	13.5	V	
	VGH	(16)	21	(26)	V	
	VGL	(-13)	-8	(-3)	V	
Input signal voltage	VCOM	-	3.7	-	V	
Logic Low input voltage	V_{IL}	0	-	$0.3 * VDD$	V	
Logic High input voltage	V_{IH}	$0.7 * VDD$	-	VDD	V	
Logic Low output voltage	V_{OL}	-	-	GND+0.4		
Logic High output voltage	V_{OH}	VDD-0.4	-	-		
Current Consumption All Black	Logic Analog	$I_{CC+} I_{IN}$	-	TBD	-	mA

*Note 1: All of the voltage listed above are with respect to GND = 0v

*Note 2: Device is subject to be damaged permanently if stresses beyond those absolute maximum rating listed above.

3.2.2 Backlight Unit

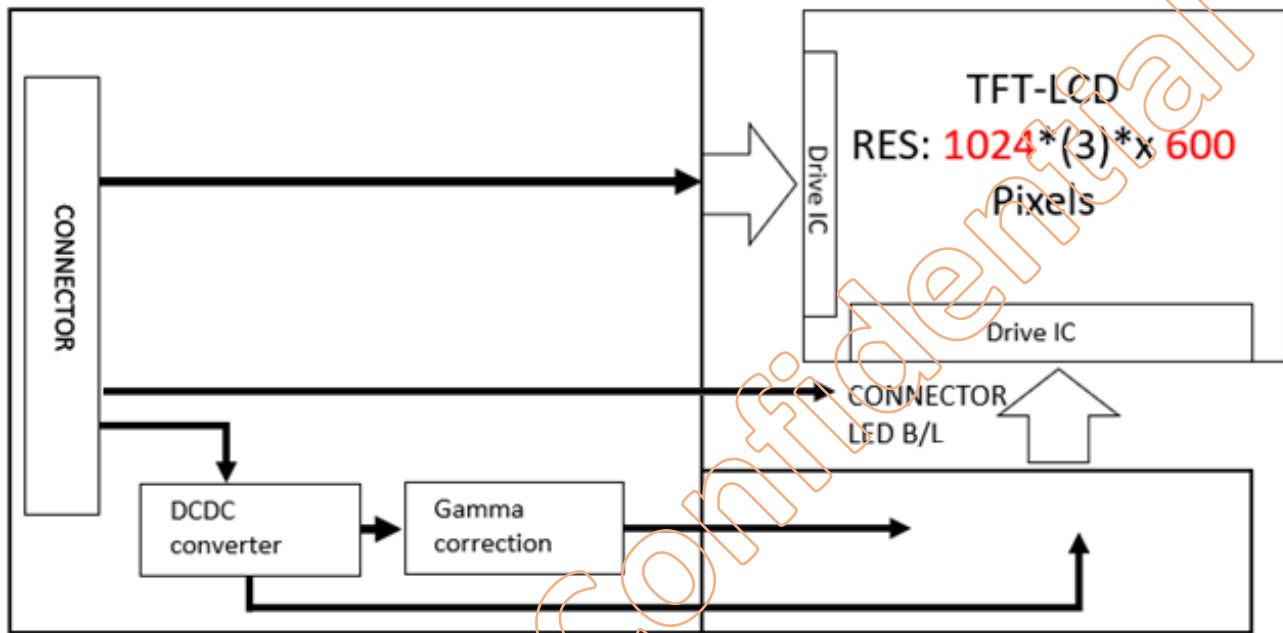
Item	Symbol	Condition	Min.	Typ.	Max	Unit
Forward Voltage	V _F	T _a =25 °C, I _F =20mA/LED	8.4	9.3	10.2	V
Forward Current	I _F	T _a =25 °C, V _F =3.1V/LED	-	200	-	mA
Power dissipation	P _D	-	-	1860	-	mW
Uniformity	Avg	-	-	80	-	%
LED working life(25°C)	-	-	-	40000	-	Hrs
Drive method	Constant current					
LED Configuration	30 White LEDs (3 LEDs in one string and 10 groups in parallel)					

* Note1 : Led life time defined as follows: The final brightness is at 50% of original brightness.

The environmental conducted under ambient air flow, at T_a=25±2 °C, 60%RH±5%, Typical operating life time is estimated data, led power dissipation is evaluated by led supplier

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4. BLOCK DIAGRAM



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5. PIN CONNECTIONS

No.	Symbol	Function
1	VCOM	Common Voltage.
2	VDD	Power Supply
3	VDD	Power Supply
4	NC	No connection.
5	GRB	Global reset pin.
6	STBYB	Standby mode, Normally pulled high. STBYB="1", all the function are on. STBYB="0", TCON and source driver are off and all output are GND.
7	GND	Ground.
8	R0N	-LVDS differential data input.
9	R0P	+LVDS differential data input.
10	GND	Ground.
11	R1N	-LVDS differential data input.
12	R1P	+LVDS differential data input.
13	GND	Ground.
14	R2N	-LVDS differential data input.
15	R2P	+LVDS differential data input.
16	GND	Ground.
17	RXCLKN	-LVDS differential clock input.
18	RXCLKP	+LVDS differential clock input.
19	GND	Ground.
20	R3N	-LVDS differential data input.
21	R3P	+LVDS differential data input.
22	GND	Ground.
23	NC	No connection.
24	NC	No connection.
25	GND	Ground.
26	NC	No connection.
27	DIMO	Backlight CABC controller signal output
28	HSD	6/8bit mode select If LVDS input data is 6bit, HSD must be set to High. If LVDS input data is 8bit, HSD must be set to Low.

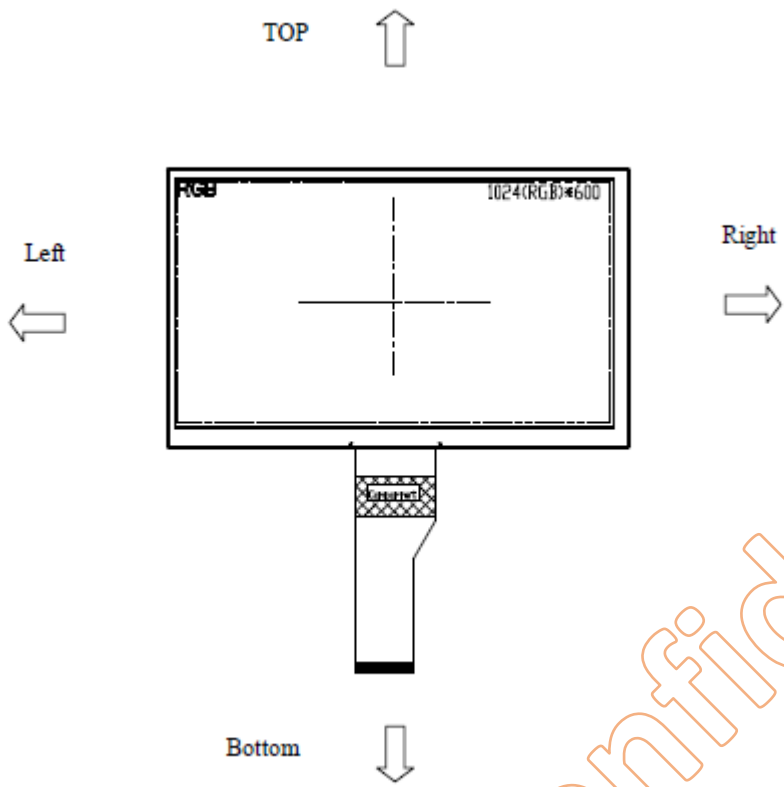
29	AVDD	Power for Analog Circuit.	
30	GND	Ground.	
31	LEDK	LED Cathode	
32	LEDK	LED Cathode	
33	L/R	Source Driver internal shift register is controlled by this pin as shown below: Normally pull high.	Note 2
34	U/P	Gate Driver UP/DOWN scan setting. Normally pull low.	Note 2
35	VGL	Gate OFF Voltage.	
36	CABCEN1	CABC H/W enable	Note 1
37	CABCEN0	CABC H/W enable	Note 1
38	VGH	Gate ON Voltage.	
39	LEDA	LED Anode	
40	LEDA	LED Anode	

Note 1:

When CABC_EN="00", CABC OFF.
 When CABC_EN="01", user interface image.
 When CABC_EN="10", still picture.
 When CABC_EN="11", moving image.

Note 2:

When L/R="0", set right to left scan direction.
 When L/R="1", set left to right scan direction.
 When U/D="0", set top to bottom scan direction.
 When U/D="1", set bottom to top scan direction.



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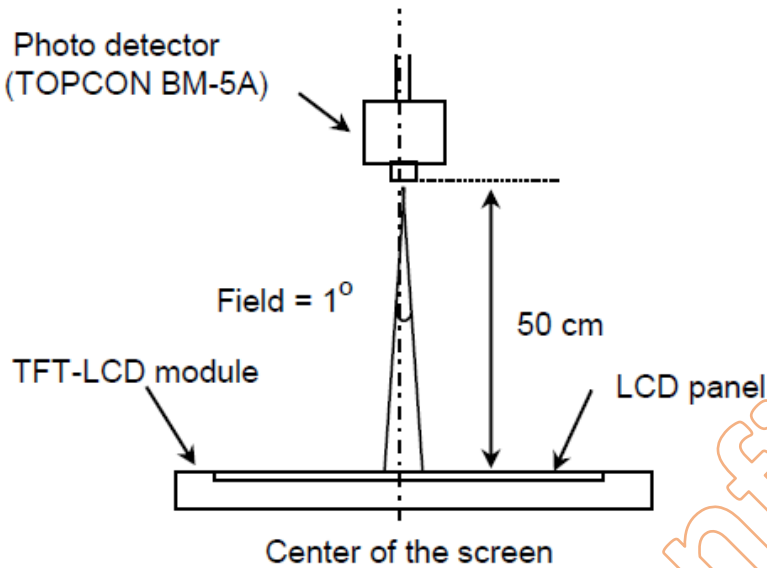
6. OPTICAL CHARACTERISTIC

6.1 Optical Characteristics

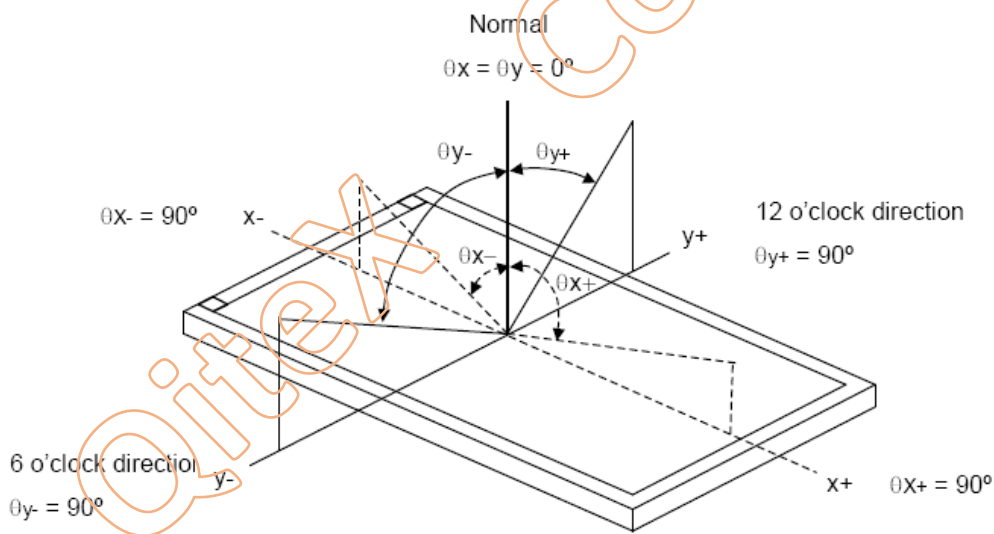
Ta=25°C, DVDD=3.3V, TN LC+ Polarizer

Item		Symbol	Condition	Specification			Unit	Note
				Min.	Typ.	Max.		
Viewing Angle	Horizontal	$\theta X+$	Center CR \geq 10	60	70	-	Deg.	Note 2
		$\theta X-$		60	70	-		
	Vertical	$\phi Y+$		50	60	-		
		$\phi Y-$		60	70	-		
NTSC Ratio(Gamut)				-	52	-	%	
Contrast ratio		CR		400	450	-		Note 3
Luminance on TFT($I_f=20mA/LED$)		Lv	Normally viewing angle $\theta X = \phi Y = 0^\circ$	320	400	-	cd/m ²	
Response time		TR+TF		-	8	-	ms	Note 4
Color Chromaticity	Red	XR			TBD		-	
		YR			TBD			
	Green	XG			TBD			
		YG			TBD			
	Blue	XB			TBD			
		YB			TBD			
	White	XW			TBD			
		YW			TBD			

* Note 1: The method of optical measurement:



* Note 2: Definition of Viewing Angles:



* Note 3: Definition of Contrast ratio

Contrast is measured perpendicular to display surface in reflective and transmissive mode.

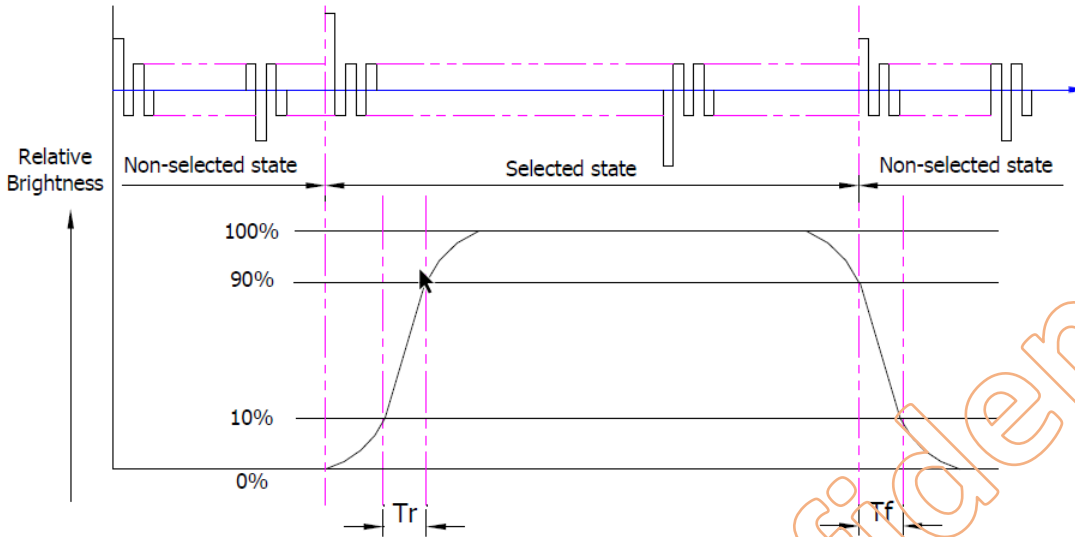
The measurement condition is:

Measuring Equipment	Eldim or Equivalent
Measuring Point Diameter	3mm//1mm
Measuring Point Location	Active Area centre point
Test pattern	A: All Pixels white
	B: All Pixel black
Contrast setting	Maximum

Definitions: CR (Contrast) = Luminance of White Pixel / Luminance of Black Pixel

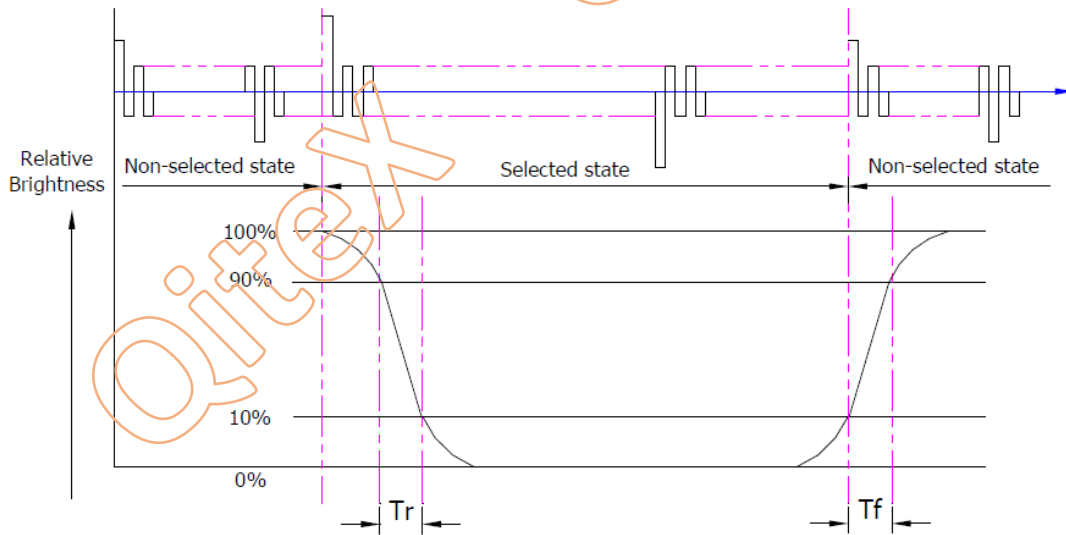
*** Note 4: Definition of Response Time:**

Normally Black Type (Negative)



- (1) T_r is the time it takes to change from non-selected stage with relative luminance 10% to selected state with relative luminance 90%.
- (2) T_f is the time it takes to change from selected state with relative luminance 90% to non-selected state with relative luminance 10%.

Normally White Type (Positive)



- (1) T_r is the time it takes to change from non-selected stage with relative luminance 90% to selected state with relative luminance 10%.
- (2) T_f is the time it takes to change from selected state with relative luminance 10% to non-selected state with relative luminance 90%;

* Measuring machine: LCD-5100 or EQUI

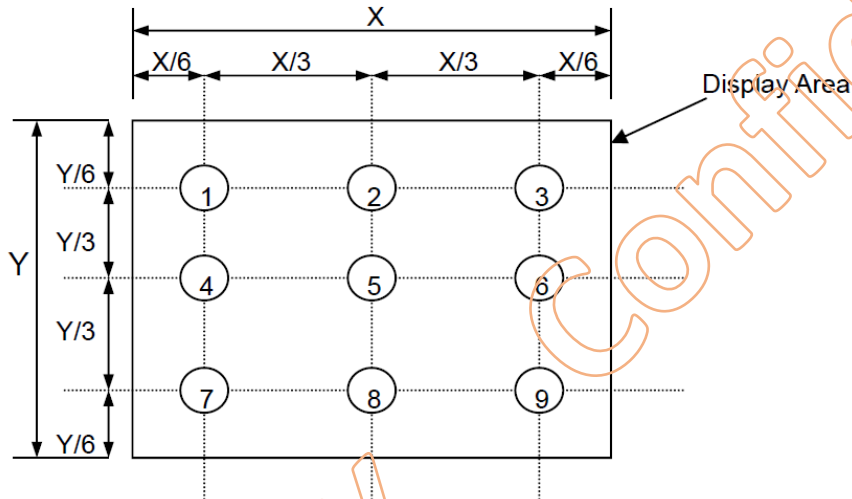
* Note 5: Definition of Surface Luminance, Uniformity and Transmittance

Using the transmissive mode measurement approach, measure the white screen luminance of the display panel and backlight.

5.5.1. Surface Luminance: $LV = \text{average (LP1:LP9)}$

5.5.2. Uniformity = $\text{Minimal (LP1:LP9) / Maximal (LP1:LP9) * 100\%}$

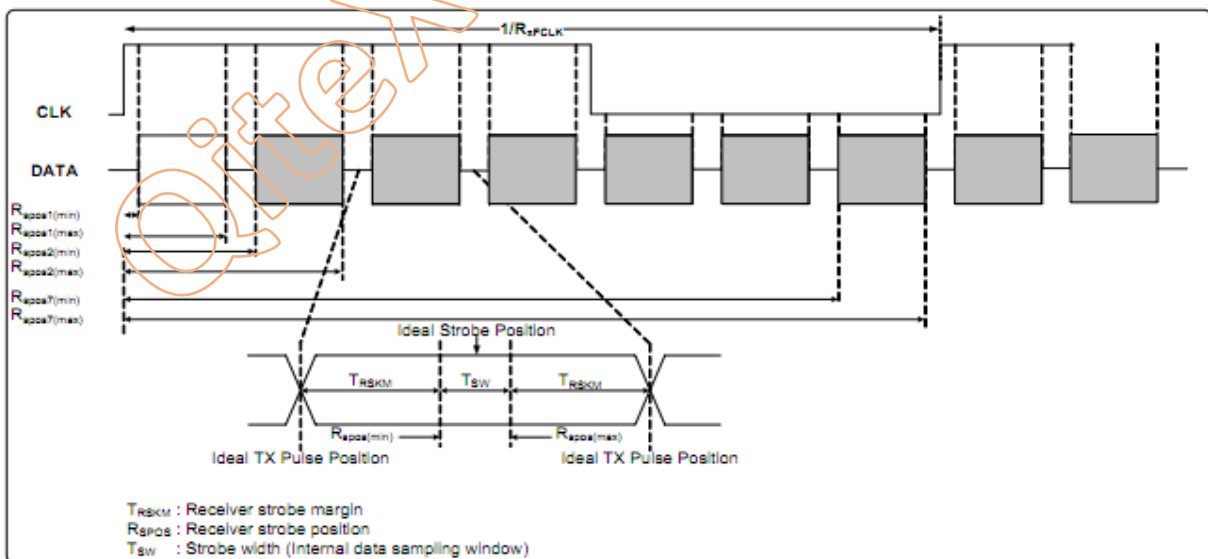
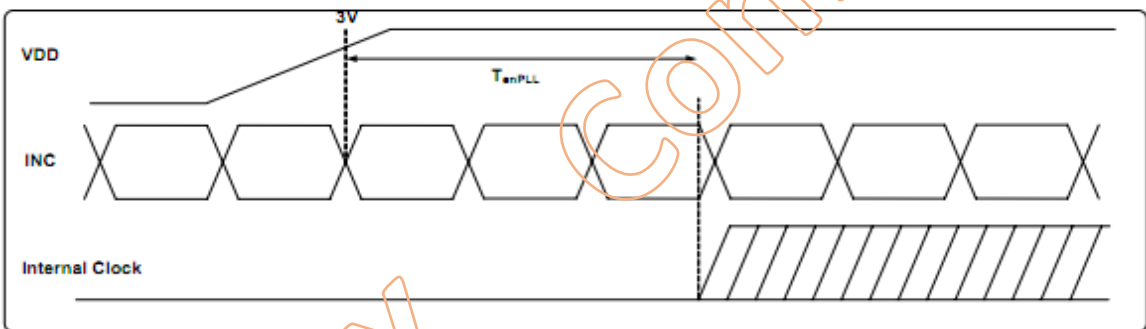
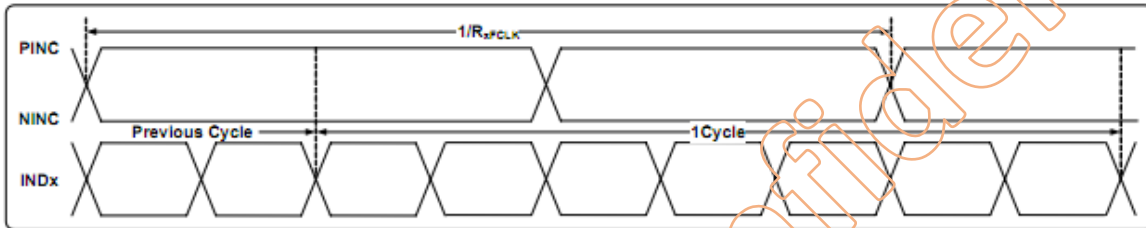
5.5.3. Transmittance = $LV \text{ on LCD} / LV \text{ on Backlight} * 100\%$



7. SIGNAL CHARACTERISTICS

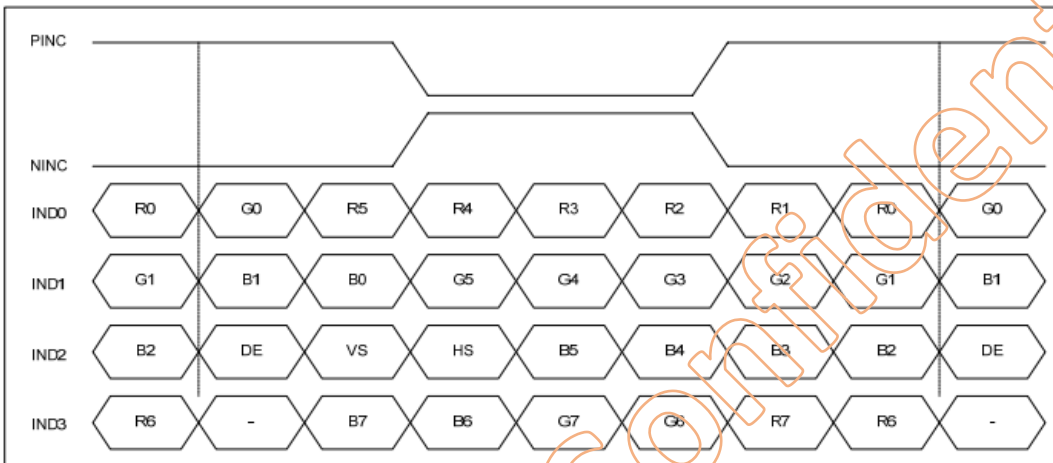
7.1 LVDS mode AC electrical characteristics

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Clock frequency	R _{XFLK}	20	-	71	MHz
Input data skew margin	T _{RSKM}	500	-	-	ps
Clock high time	T _{LVCH}	-	4/(7* R _{XFLK})	-	ns
Clock low time	T _{LVCL}	-	3/(7* R _{XFLK})	-	ns
PLL wake-up time	T _{emPLL}	-	-	150	us

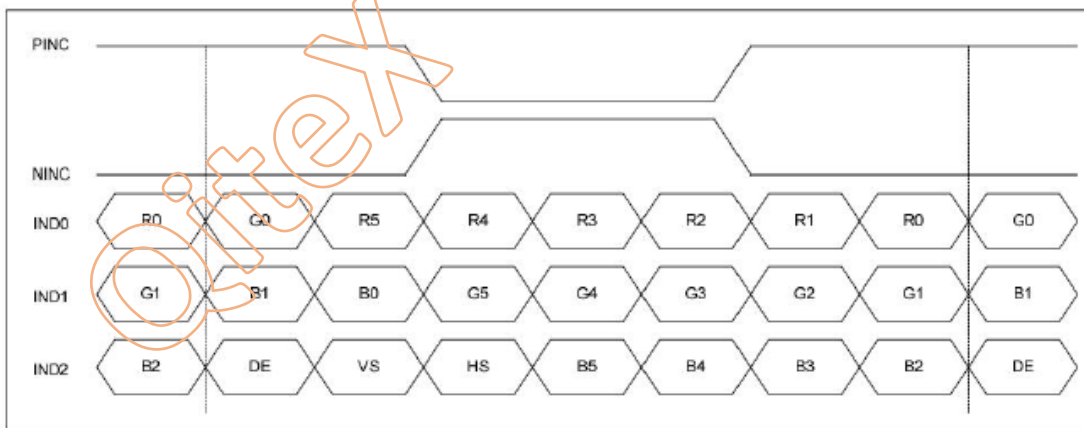


Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Modulation Frequency	SSC _{MF}	23	-	93	KHZ
Modulation Rate	SSC _{MR}	-	-	+/- 3	LVDS clock = 71MHz center spread

7.1.1 Data input format



8-bit LVDS input



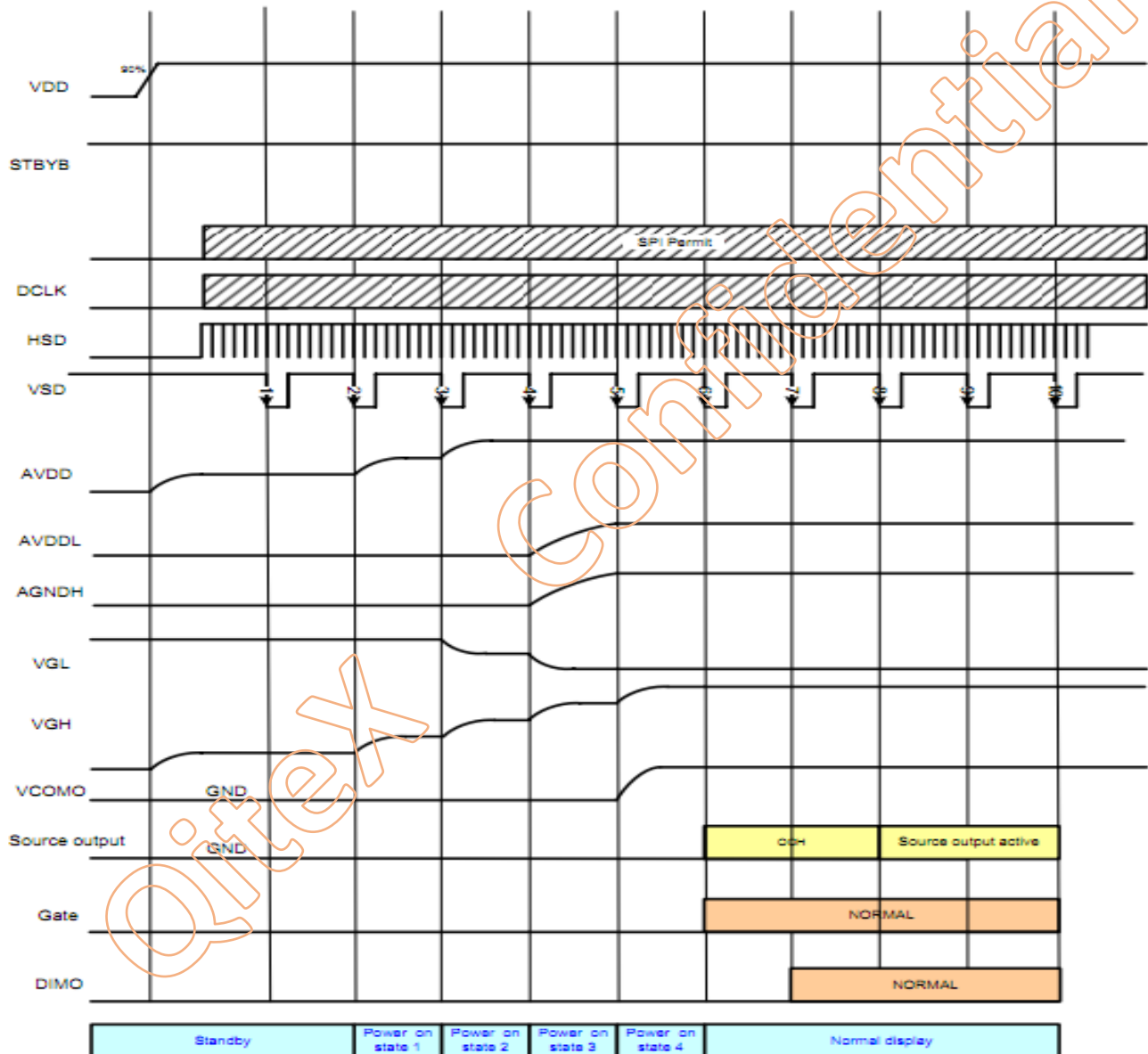
6-bit LVDS input

7.2 Power On/Off Sequence

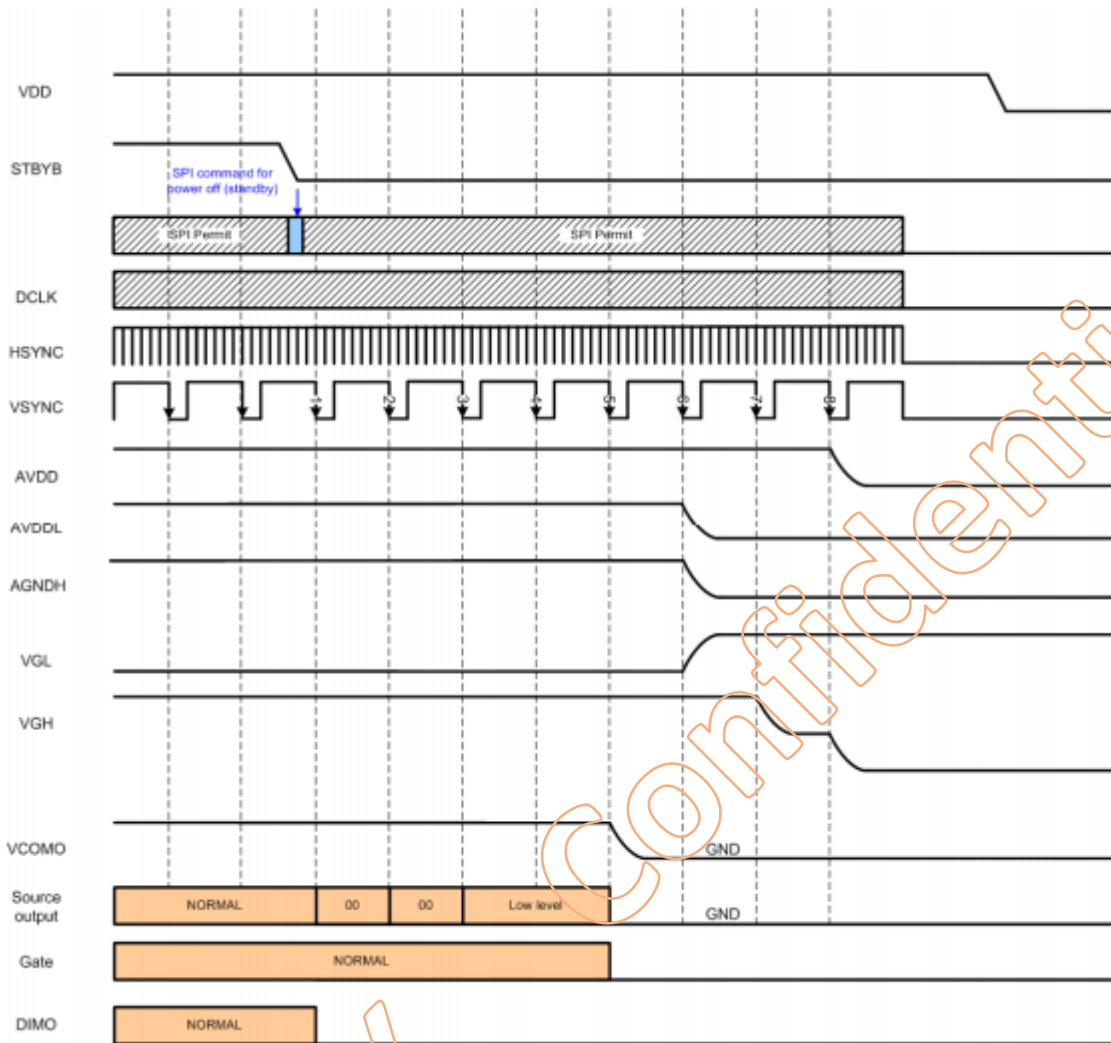
To prevent the device damage from latch up, the power on/off sequence shown below must be followed.

Power on: VDD, GND → AVDD, AGND → V1 to V14

Power off: V1 to V14 → AVDD, AGND → VDD, GND



Power on timing sequence



Power off timing sequence

8. UTLINE DRAWING

