MES2L484 Series Development Board

Hardware User Manual V1.0

Unisplendour Logos2 Series FPGA

Development Platform

Version Date : 2024-06-06

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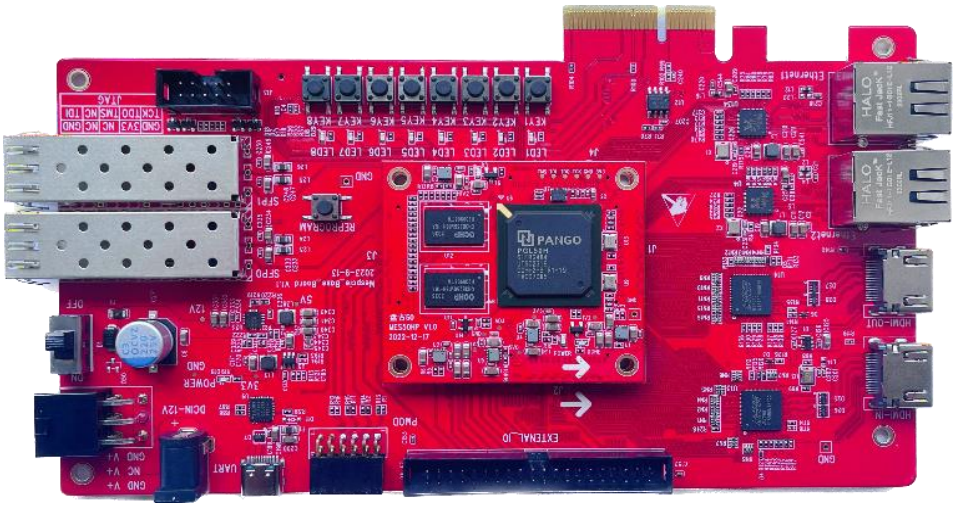
1. Development system introduction

1.1 Development System Overview

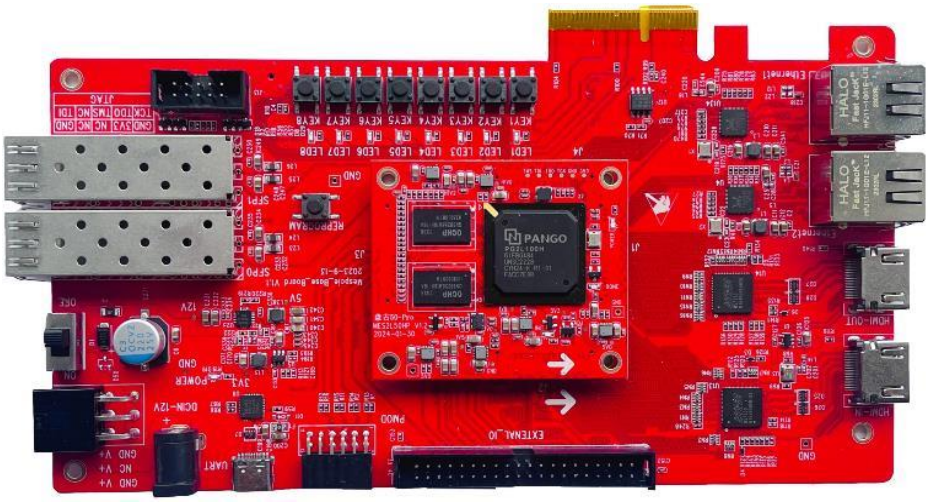
The MES2L484 series development board (MES2L484-50AG, MES2L484-100AG, MES2L484-200AG) adopts the structure of core board + expansion board, and the core board and expansion board are connected by high-speed board-to-board connector. This series of boards use the same expansion board, but the MES2L484-50AG development board does not support the expansion board 40pin expansion port. The manual is shown with MES2L100AG diagram, and the diagram is applicable to MES2L484-50AG and MES2L484-200AG.

The core board is mainly composed of FPGA+2 DDR3+Flash+power supply and reset, which undertakes the minimum system operation and high-speed data processing and storage functions of FPGA. This series of FPGAs uses the FPGAs of Unigroup Tongchuang's 28nm process (Logos2 series: PG2L50H-6IFBG484, PG2L100H-6IFBG484, PG2L200H-6IFBB484); among them, the MES2L484-50AG is equipped with the FPGA model: PG2L50H-6IFBG484, the MES2L484-100AG is equipped with the FPGA model: PG2L100H-6IFBG484, and the MES2L484-200AG is equipped with the FPGA model: PG2L200H-6IFBB484.

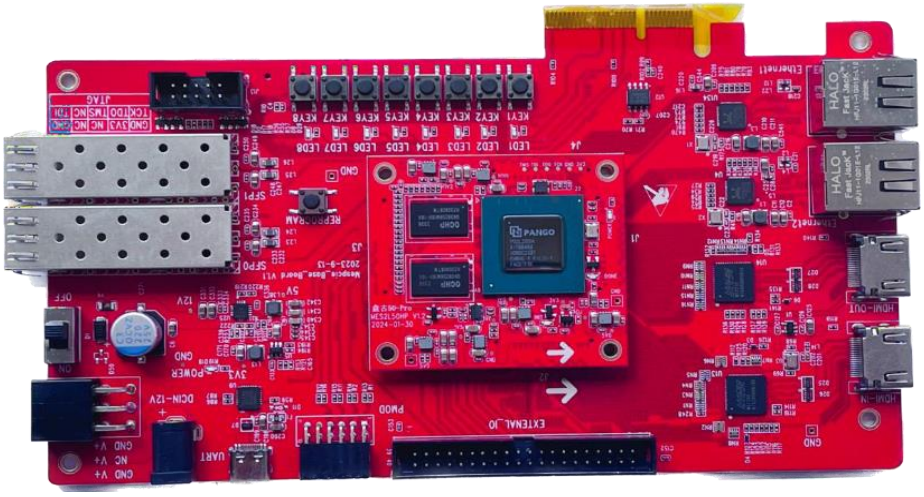
The data exchange clock frequency between PG2L50H, PG2L100H, PG2L200H and DDR3 on the core board is up to 533MHz, the data bit width of 2 DDR3 is 32bit, and the total data bandwidth is up to 34112 (1066×32) Mbps, which can meet the needs of users for high-speed multi-channel data storage. In addition, PG2L50H, PG2L100H, and PG2L200H are equipped with 4 HSST high-speed transceivers, each with a speed of up to 6.6Gbps, which are used for optical fiber communication and PCIe data communication. The power supply solution is implemented using multiple EZ8303 (Aino). The baseboard expands the core board with a variety of peripheral interfaces, including the HDMI transceiver interface for the transmission of video image data; the optical fiber interface, 10/100/1000M Ethernet interface, and PCIE interface are convenient for the verification of various high-speed communication systems; a 40-pin IO expansion connector and a PMOD expansion connector are reserved for users to verify various peripheral devices.



MES2L484-50AG Development Board



MES2L484-100AG Development Board

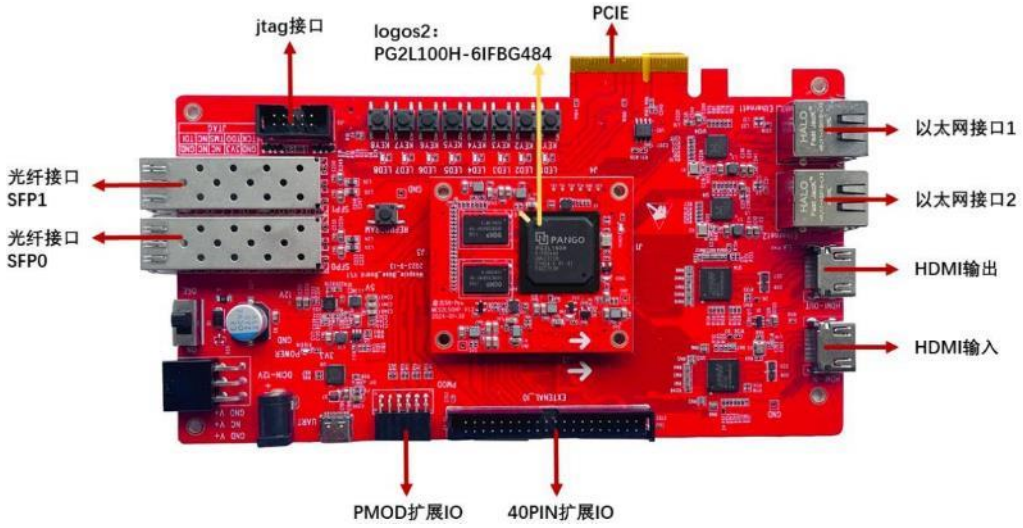


MES2L484-200AG Development Board

1.2 Development System Introduction

1.2.1 Development system peripheral resources

- HDMI Input interface *1
- HDMI Output interface *1
- Optical fiber interface *2
- 10/100/1000M Ethernet interface *2
- PCIE X2 Interface *1
- Jtag Debug interface *1
- SD Card interface *1
- PMOD interface *1
- IO Expansion port *1
- USB Serial port *1
- Buttons *8
- LEDs *8



1.2.2 Development system functional block diagram

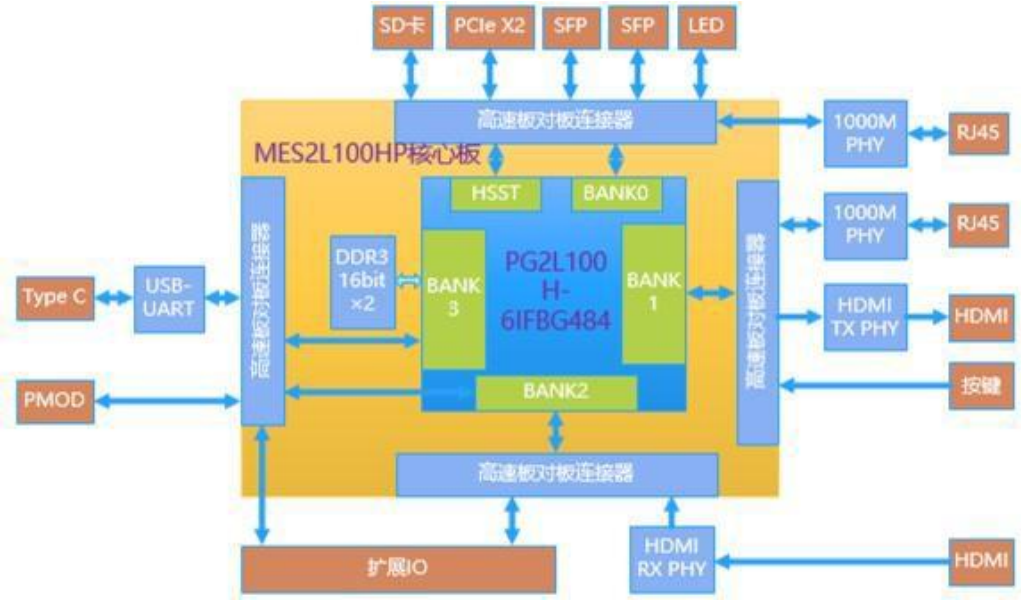


Figure 1-1 MES2L484 Series Development System Functional Block Diagram

The functional details of the MES2L484 series development platform are as follows:

- Logos2 FPGA core board

It consists of PG2L50H/PG2L100H/PG2L200H+2 512MB DDR3+128MB QSPI FLASH. In addition, there is a high-precision 27MHz single-ended crystal oscillator and two 125MHz differential crystal oscillators on the board to provide stable clock input for the FPGA system and high-speed serial transceiver HSST module.

- 10/100M/1000M Ethernet RJ-45 interface *2

The network port PHY chip uses RTL8211E, which supports 10/100M/1000Mbps network transmission data rate; supports full-duplex working mode and data rate adaptation.

- PCIe X2 interface * 1

Supports PCI Express 2.0 standard, provides PCIe X2 high-speed data transmission interface, and the single-channel communication rate can be up to 5GBaud.

- SFP high-speed fiber interface * 2

The 2 high-speed transceivers of the HSST transceiver of the Logos2 FPGA are connected to the transmission and reception of 2 optical modules to realize 2 high-speed

fiber communication interfaces. The receiving and transmitting speed of each fiber data communication is up to 6.6Gb/s.

- HDMI output * 1

The MS7210 HMDI transmission chip of the domestic Hongjing Micro Company is selected, which is compatible with HDMI1.4b and the 3D transmission format of standard video under HDMI 1.4b. The highest resolution supported is up to 4K@30Hz, and the highest sampling rate is up to 300MHz; HBR audio is supported.

- HDMI input * 1

The MS7200 HMDI receiving chip of the domestic Hongjing Micro Company is selected, which is compatible with HDMI1.4b and the 3D transmission format of standard video under HDMI 1.4b. The highest resolution supported is up to 4K@30Hz, and the highest sampling rate is up to 300MHz; HBR audio is supported.

- USB to Serial Port * 1

Used for serial communication with the computer, convenient for users to debug. The serial port chip uses SiliconLabs' USB-UART chip: CP2102, and the USB interface uses USB Type C interface.

- Micro SD Card Holder

Supports SDIO mode and SPI mode.

- EEPROM

Onboard IIC interface EEPROM: 24C02;

- JTAG interface

10-pin 2.54mm pitch double-row pin header, used for downloading and debugging FPGA programs.

- PMOD Seat

Reserve 1 12-pin (2×6) PMOD interface.

- 40-pin expansion port

Reserve 1 40-pin 2.54mm pitch expansion port, which can be connected to various modules. The expansion port includes 1 5V power supply, 2 3.3V power supplies, 3 grounds, and 34 I/O ports.

Note: The MES2L484-50AG development board does not support the use of the 40-pin expansion port.

- LED lights

8 user LEDs;

- Buttons

2. Core board

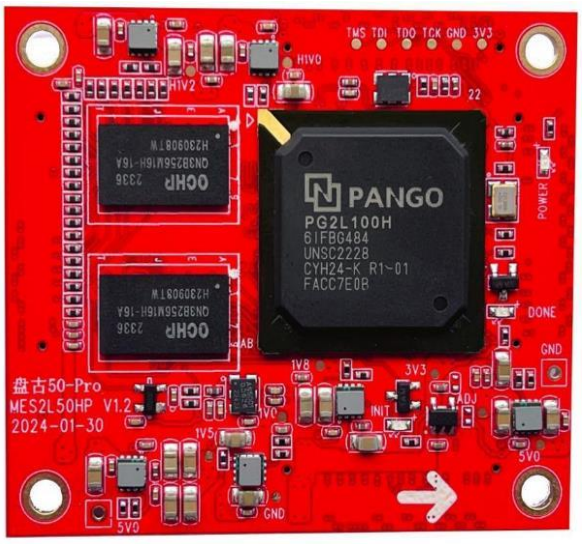
2.1 Core Board Overview

The MES2L484 series core board is a new domestic high-performance FPGA core board developed by "Xiaoyan Technology" based on many years of FPGA development experience, using the Unigroup Tongchuang logos2 series PG2L50H-6IFBG484\ PG2L100H-6IFBG484\PG2L200H-6IFBB484 as the main control chip. It has the characteristics of high data bandwidth and high storage capacity, and is suitable for multiple application scenarios such as video image processing, high-speed data acquisition, and industrial control.

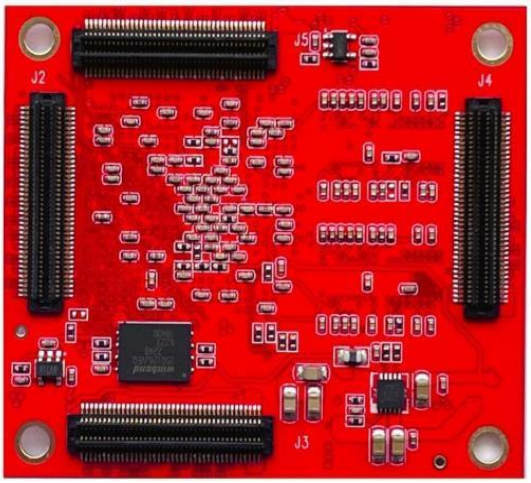
The MES2L484 series core board uses 2 DDR3 chips, with a total capacity of 8Gbit, a combined data bus width of 32bit, and a maximum rate of 1066Mbps, which meets the user's high-bandwidth data processing needs.

The MES2L484 series core board power supply adopts Aino DCDC and Nanjing Weimeng LDO solutions, and QSPI FLASH uses Winbond's W25Q128 chip with a capacity of 128Mb, which is used to store FPGA startup files.

The MES2L484 series core board has a size of 50*58mm. It not only expands 3.3V common IO and 1.5V common IO, but also expands 1 pair of ADC interfaces, 1 group of JTAG interfaces, 4 pairs of HSST high-speed RX/TX differential signals and 1 pair of HSST high-speed interface reference input clock. While meeting the user's large number of IO requirements, the routing between the FPGA chip and the interface is equal length and differential, which is very suitable for secondary development.



MES2L484 Front side of series core board



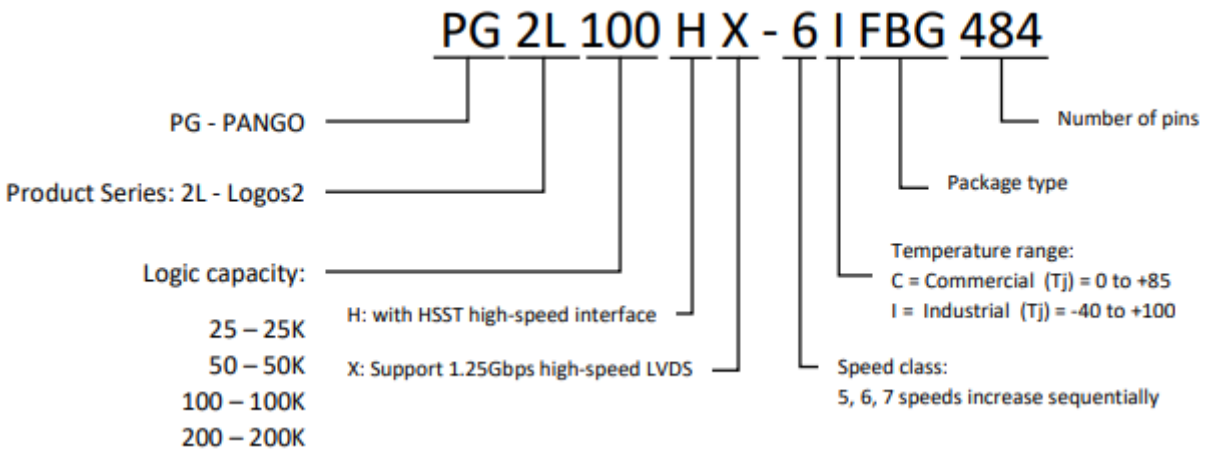
MES2L484 Back side of series core board

2.2 System specification

2.2.1 FPGA

FPGA models PG2L50H-6IFBG484, PG2L100H-6IFBG484, and PG2L200H-6IFBB484 all belong to the Unigroup Tongchuang Logos2 series of products, with a speed grade of 6, a temperature range of industrial grade (-40~100℃), and a pin count of 484. PG2L50H-6IFBG484 and PG2L100H-6IFBG484 are packaged as FBG.

The numbering content and meaning of Unigroup Tongchuang Logos2 series FPGA product models are as follows:



The main parameters of PG2L50H-6IFBG484 are as follows:

Resource		Parameter
Logical resources	Flip-flop (FF)	71600
	LUT6	35800
	Equivalence LUT4	53700
RAM resource	Distributed RAM (Kbit)	593.75
	Block RAM Quantity (36K/ block)	85
	Block RAM (Kbit)	3060
Clock Resources	GPLL	5
	PPLL	5
Hardcore resources	APM (25*18 Multiplier	120
	ADC	1
	AES	1
	HSST (6.6G)	4
	PCIE Gen2*4	1
IO resource	User IO	250

The main parameters of PG2L100H-6IFBG484 are as follows:

Resource		Parameter
Logical resources	Flip-flop (FF)	133200
	LUT6	66600
	Equivalence LUT4	99900
RAM resource	Distributed RAM (Kbit)	1243.75
	Block RAM Quantity (36K/ block)	155
	Block RAM (Kbit)	5580
Clock Resources	GPLL	6
	PPLL	6
Hardcore resources	APM (25*18 Multiplier	240
	ADC	1
	AES	1

	HSST (6.6G)	4
	PCIE Gen2*4	1
IO resource	User IO	285

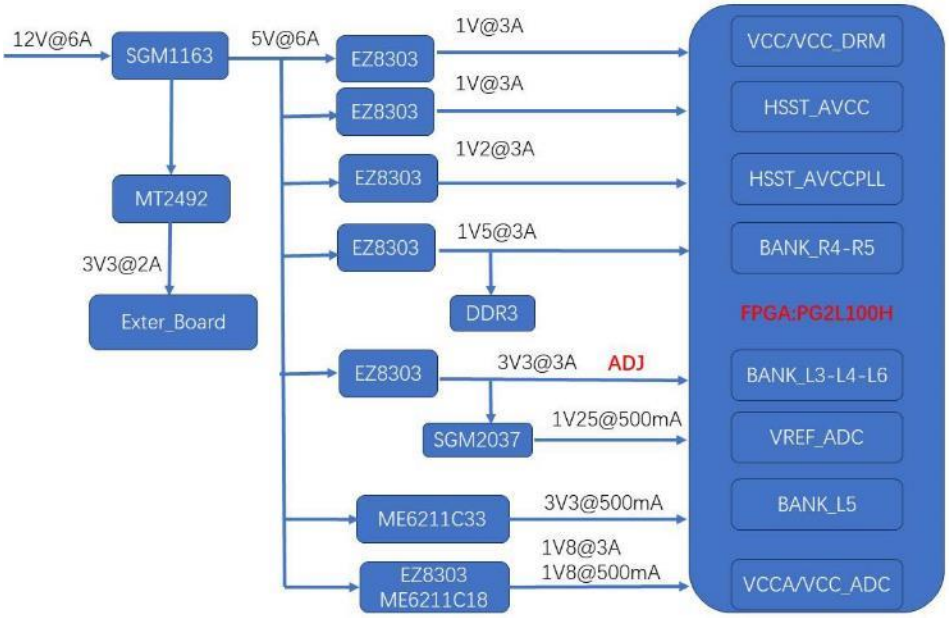
The main parameters of PG2L200H-6IFBB484 are as follows:

Resource		Parameter
Logical resources	Flip-flop (FF)	319600
	LUT6	159800
	Equivalence LUT4	239700
RAM resource	Distributed RAM (Kbit)	2468.75
	Block RAM Quantity (36K/ block)	415
	Block RAM (Kbit)	14940
Clock Resources	GPLL	10
	PPLL	10
Hardcore resources	APM (25*18 Multiplier	740
	ADC	1
	AES	1
	HSST (6.6G)	4
	PCIE Gen2*4	1
IO resource	User IO	285

2.2.2 Power interface

The power supply voltage of the MES2L484 series core board is VCCIN, and the input voltage is 5V. It needs to be powered through the board-to-board connector. When connected to the baseboard, it is powered through the baseboard. The power design diagram on the board is shown below:

The power supply network of the system is as follows:



The functions of each power supply rail is as follows :

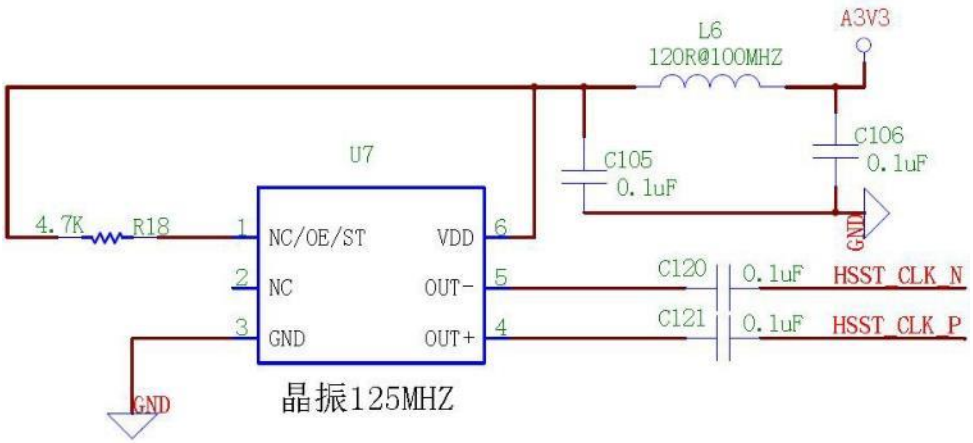
Power supply	Functional purpose
5.0V	Low voltage DC-DC Power supply ;
1.0V	VCC Core voltage ;
HSST_1.0V	PG2L484 series HSST Transceiver channel and phase-locked loop power supply
1.5V	DDR3 Supply voltage and Bank R4 , Bank R5 power supply ;
1.8V	Auxiliary power
3.3V	I/O Voltage, supply voltage of some interfaces (crystal oscillator , FLASH)
VTT(0.75V)	DDR3 Pull-up voltage on control and address lines to maintain signal integrity ;
VREF(0.75V)	DDR3 Reference voltage ;

2.2.3 Clock

The MES2L484 series core board is equipped with two 125MHz active differential crystal oscillators and one single-ended 27MHz crystal oscillator. One 125MHz differential crystal oscillator is used as the reference clock input of the HSST transceiver, and the other 125MHz differential crystal oscillator and 27MHz single-ended crystal oscillator are used as the main clock input of the FPGA.

2.2.3.1 125MHz Differential crystal oscillator

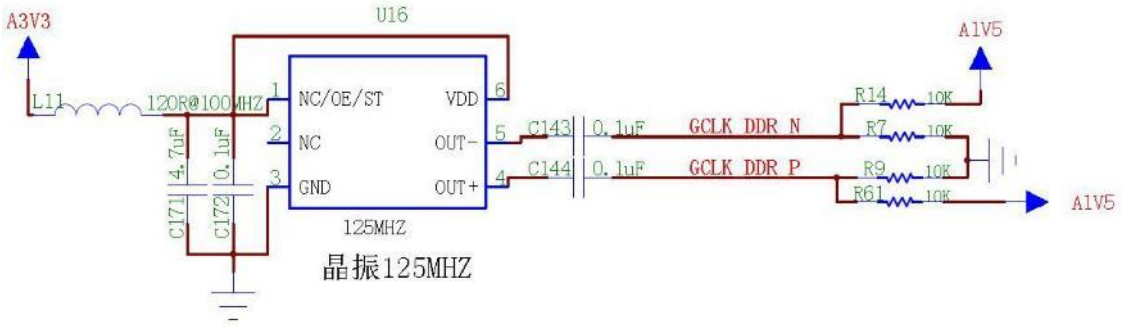
U7 in the figure below is a 125MHz active differential crystal oscillator circuit, which is the reference input clock provided to the HSST module inside the FPGA. The crystal oscillator output is connected to the clock pin of the FPGA HSST BANK.



Please see the following table for specific pin assignments:

Signal	PG2L484 Pin name
HSST_CLK_P	F6
HSST_CLK_N	E6

The figure below shows a 125MHz active differential crystal oscillator circuit. This clock provides clock input to the logic inside the FPGA and can be used for logic design or to generate clocks of different frequencies through PLL.

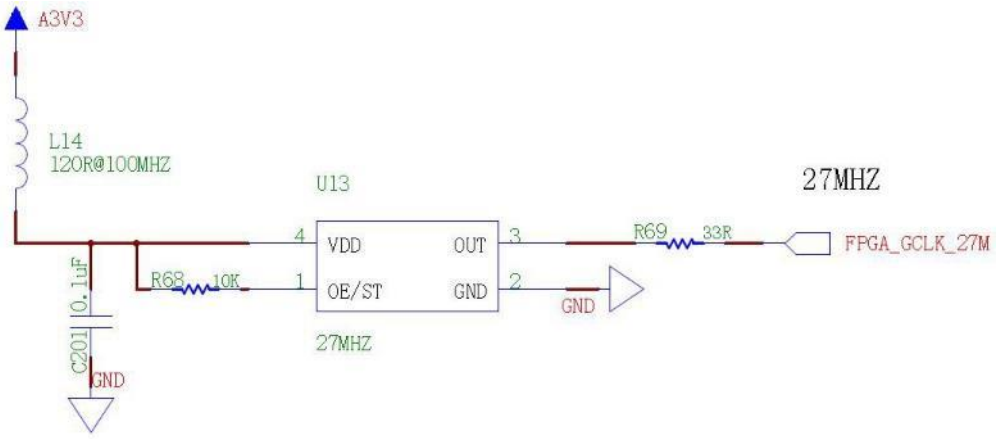


Please see the following table for specific pin assignments :

Signal	PG2L484 Pin name
GCLK_DDR_P	V4
GCLK_DDR_N	W4

2.2.3.2 27MHz Single-ended crystal oscillator

The figure below shows an active single-ended crystal oscillator circuit, which is provided to the logic clock input inside the FPGA and can be used for logic design or to generate clocks of different frequencies through PLL.



Please see the following table for specific pin assignments :

Signal	PG2L484 Pin name
FPGA_GCLK_27M	Y18

2.2.4 Power on IO Status

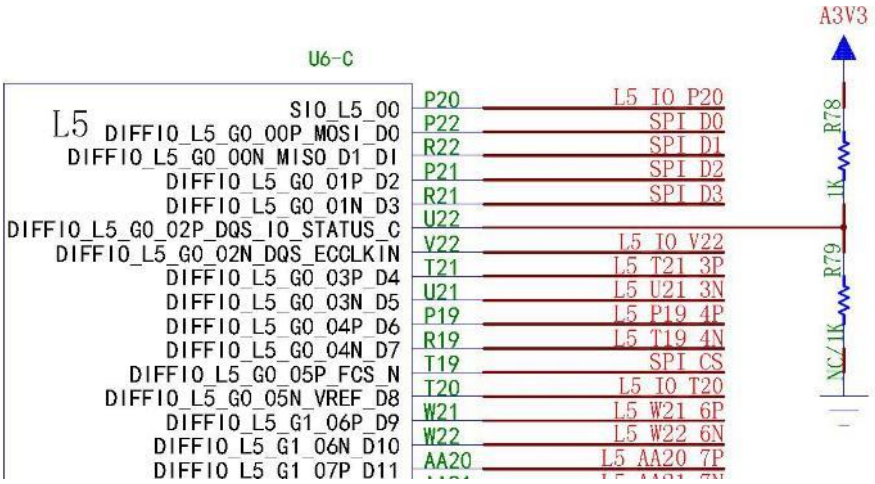
There is a function multiplexing IO on the Logos2 device, which controls whether the weak pull-up resistors of all user IOs are enabled from the completion of power-on to the entry into user mode. This pin is not allowed to be left floating before or during configuration. The corresponding functions of this IO after power-on are as follows:

(1) "0", enable all user IO internal pull-up resistors.

(2) "1", do not enable all user IO internal pull-up resistors.

The MES2L484 series core board connects this pin to GND by default. Users can select the initial IO state after power-on by soldering resistors according to their needs;

The functional circuit is as follows:

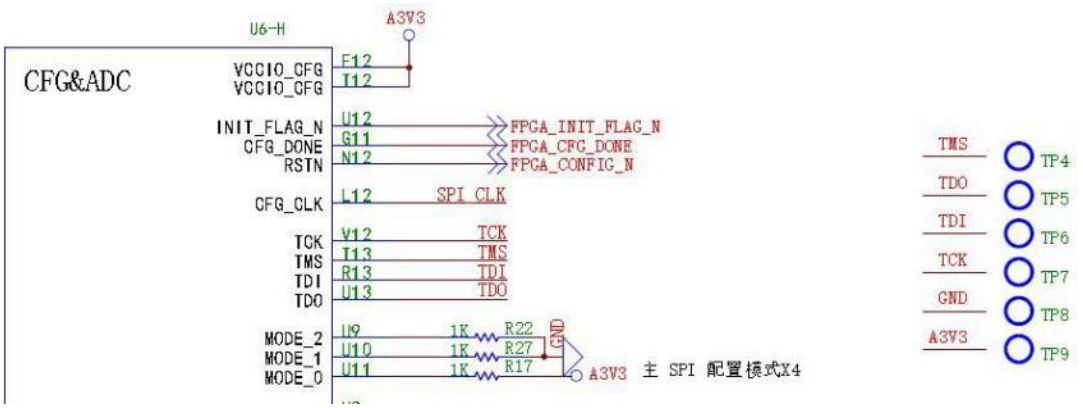


IO Status Configuration Circuit

2.2.5 JTAG interface

The MES2L484 series core board has a reserved JTAG contact in the upper left corner of the front, which can be used to debug the core board without a baseboard. The FPGA's JTAG signal is connected to the baseboard JTAG interface through a high-speed board-to-board connector, which is used to download the FPGA program or fix the program to FLASH.

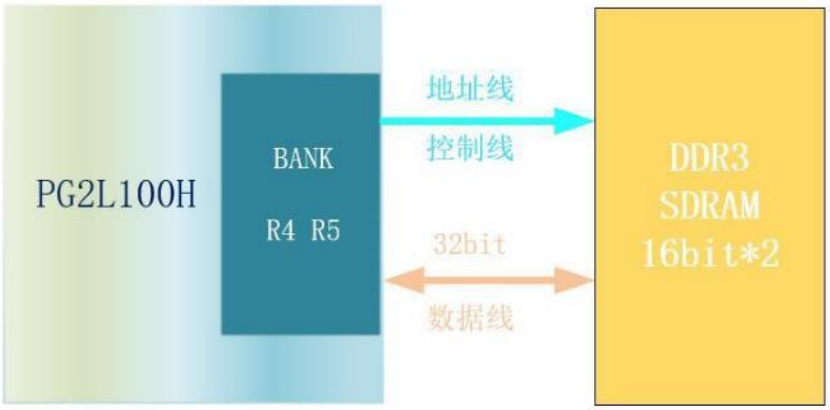
The upper right corner of the front of the MES2L484 series core board



JTAG Interface Circuit

2.2.6 DDR3

The MES2L484 series core board is equipped with two Micron 4Gbit (512MB) DDR3 chips (8Gbit in total), model MT41K256M16TW-107:P (compatible with MicronMT41K256M16HA-125, Winbong W634GU6NB-11). The bus width of DDR is 32bit in total. The maximum operating clock speed of DDR3 SDRAM can reach 533MHz (data rate 1066Mbps). The DDR3 storage system is directly connected to BANK R4 R5 of FPGA. Matching resistors/terminal resistors, trace impedance control, and trace equal length control have been fully considered in circuit design and PCB design to ensure high-speed and stable operation of DDR3. The hardware connection diagram of DDR3 DRAM is shown in the figure below:



DDR3 routing uses 50 ohm trace impedance for single-ended signals, DCI resistors (VRP/VRN) and differential clocks are set to 100 ohms. Each DDR3 chip uses a 240 ohm resistor pull-down on ZQ. DDR-VDDQ is set to 1.5V to support the selected DDR3 device. DDR-VTT is always voltage following DDR-VDDQ, maintaining a voltage value of 1/2 times DDR-VDDQ. DDR-VREF is an independent buffer output equal to 1/2 times the voltage of DDR-VDDQ. DDR-VREF is isolated to provide a clearer reference for DDR level conversion.

The specific pin allocation of DDR3 is as follows::

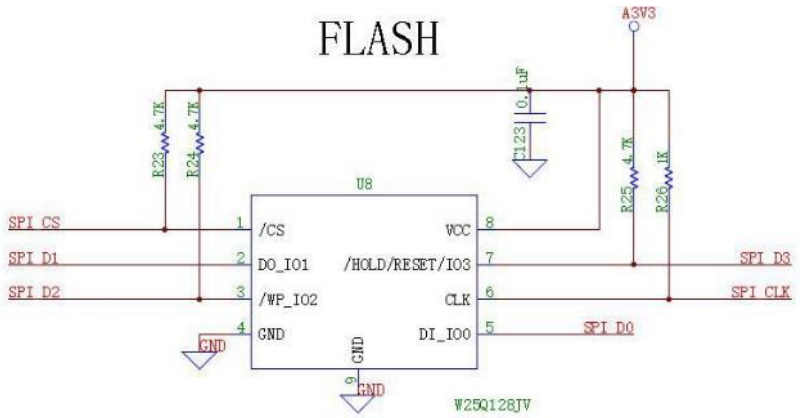
Signal name	PG2L484 Pins	Signal name	PG2L484 Pins
ddr3_addr[0]	Y6	ddr3_addr[14]	AA1
ddr3_addr[1]	AA5	ddr3_addr[15]	AB1
ddr3_addr[2]	Y3	ddr3_ba[0]	W2
ddr3_addr[3]	W1	ddr3_ba[1]	AB5
ddr3_addr[4]	AB6	ddr3_ba[2]	Y7
ddr3_addr[5]	U1	ddr3_cas_n	W6
ddr3_addr[6]	AB7	ddr3_ck_n	AA4
ddr3_addr[7]	U2	ddr3_ck_p	Y4
ddr3_addr[8]	AB8	ddr3_cke	AB3
ddr3_addr[9]	Y2	ddr3_cs_n	W5
ddr3_addr[10]	AB2	ddr3_odt	V2
ddr3_addr[11]	AA3	ddr3_ras_n	AA8
ddr3_addr[12]	AA6	ddr3_reset_n	U3
ddr3_addr[13]	Y1	ddr3_we_n	Y8
ddr3_dm[0]	L5	ddr3_dm[2]	F3
ddr3_dm[1]	N2	ddr3_dm[3]	H3
ddr3_dq[0]	K4	ddr3_dq[16]	C2
ddr3_dq[1]	L4	ddr3_dq[17]	E2
ddr3_dq[2]	J6	ddr3_dq[18]	B2
ddr3_dq[3]	M3	ddr3_dq[19]	F1
ddr3_dq[4]	K3	ddr3_dq[20]	B1
ddr3_dq[5]	M2	ddr3_dq[21]	G1
ddr3_dq[6]	J4	ddr3_dq[22]	A1
ddr3_dq[7]	L3	ddr3_dq[23]	D2
ddr3_dq[8]	P1	ddr3_dq[24]	H2

ddr3_dq[9]	N4	ddr3_dq[25]	H4
ddr3_dq[10]	R1	ddr3_dq[26]	K1
ddr3_dq[11]	M5	ddr3_dq[27]	G3
ddr3_dq[12]	P2	ddr3_dq[28]	J5
ddr3_dq[13]	M6	ddr3_dq[29]	G4
ddr3_dq[14]	P6	ddr3_dq[30]	J1
ddr3_dq[15]	N5	ddr3_dq[31]	G2
ddr3_dqs_p[0]	M1	ddr3_dqs_n[0]	L1
ddr3_dqs_p[1]	P5	ddr3_dqs_n[1]	P4
ddr3_dqs_P[2]	E1	ddr3_dqs_n[2]	D1
ddr3_dqs_P[3]	K2	ddr3_dqs_n[3]	J2

2.2.7 QSPI Flash

The MES2L484 series core board uses Winbond's 4-bit SPI (QSPI) serial NOR flash memory W25Q128.

The circuit connection of QSPI is as follows:

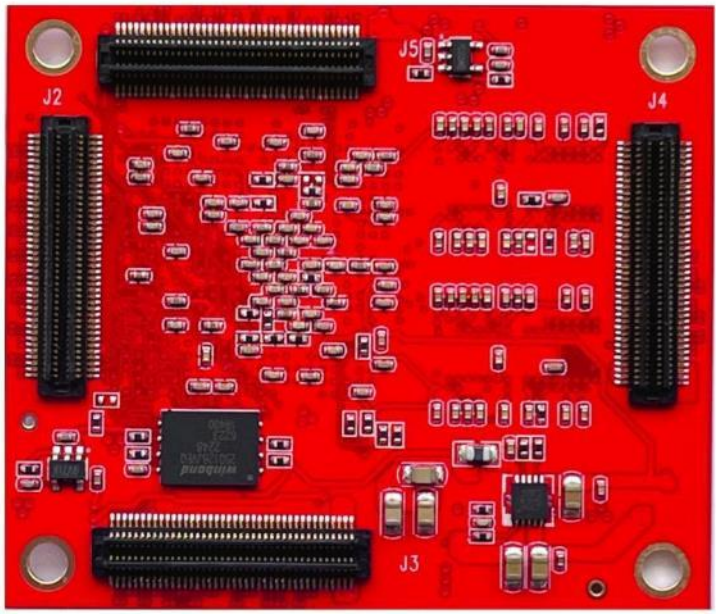


QSPI Flash pin assignments are as follows

Signal	Description	PG2L484 Pin	QSPI Pin
CS	Chip Select	T19	1
DQ	Data bits 0	P22	5
DQ1	Data bits 1	R22	2
DQ2	Data bits 2	P21	3
DQ3	Data bits 3	R21	7
SCK	Serial Data Clock	L12	6

2.2.8 Expansion IO

There are 4 80-pin high-speed expansion ports J2/J3/J4/J5 on the back of the MES2L484 series core board, with a pin spacing of 0.5mm. The FPGA's IO is connected to the baseboard through the 4 expansion ports to achieve high-speed data communication.



Expansion port J2 :

J2 Pins	Network Name	FPGA pins	J2 Pins	Network Name	FPGA Pins
1	L4_IO_M17	M17	2	L4_M18_15P	M18
3	L4_IO_J16	J16	4	L4_L18_15N	L18
5	L4_N20_17P	N20	6	L4_M15_23P	M15
7	L4_M20_17N	M20	8	L4_M16_23N	M16
9	GND		10	GND	
11	L4_N18_16P	N18	12	L4_L14_21P	L14
13	L4_N19_16N	N19	14	L4_L15_21N	L15
15	L4_N22_14P	N22	16	L4_M13_19P	M13
17	L4_M22_14N	M22	18	L4_L13_19N	L13
19	GND		20	GND	
21	L4_M21_9P	M21	22	L4_K21_8P	K21
23	L4_L21_9N	L21	24	L4_K22_8N	K22
25	L4_K18_GCLK	K18	26	L4_L19_13P	L19
27	NC		28	L4_L20_13N	L20
29	GND		30	GND	

31	NC		**32**	L4_K17_20P	K17
33	NC		**34**	L4_J17_20N	J17
35	NC		**36**	L4_L16_22P	L16
37	NC		**38**	L4_K16_22N	K16
39	NC		**40**	L4_K13_18P	K13
41	NC		**42**	L4_K14_18N	K14
43	NC		**44**	L4_J22_6P	J22
45	L5_IO_Y19	Y19	**46**	L4_H22_6N	H22
47	L5_IO_W20	W20	**48**	L4_J20_10P	J20
49	L5_IO_V22	V22	**50**	L4_J21_10N	J21
51	L5_IO_T20	T20	**52**	L4_H17_5P	H17
53	L5_IO_P20	P20	**54**	L4_H18_5N	H18
55	L5_IO_N15	N15	**56**	L4_J15_4P	J15
57	L4_J19_11P	J19	**58**	L4_H15_4N	H15
59	L4_H19_11N	H19	**60**	L4_H20_7P	H20
61	NC		**62**	L4_G20_7N	G20
63	GND		**64**	GND	
65	NC		**66**	L4_G17_3P	G17
67	NC		**68**	L4_G18_3N	G18
69	L4_G15_1P	G15	**70**	L3_IO_F21	F21
71	L4_G16_1N	G16	**72**	L3_IO_F15	F15
73	L4_J14_2P	J14	**74**	L3_G21_23P	G21
75	L4_H14_2N	H14	**76**	L3_G22_23N	G22
77	L4_H13_0P	H13	**78**	L3_F19_17P	F19
79	L4_G13_0N	G13	**80**	L3_F20_17N	F20
81	NC		**82**	NC	

Expansion port J3 :

J3 Pins	Network Name	FPGA pins	J3 Pins	Network Name	FPGA Pins
1	5V		2	5V	
3			4		
5			6		
7			8		
9	GND		10	GND	
11	/		12	GND	
13	L6_V13_12P	V13	14	L6_AA13_2P	AA13
15	L6_V14_12N	V14	16	L6_AB13_2N	AB13
17	L6_T14_14P	T14	18	L6_Y13_4P	Y13
19	L6_T15_14N	T15	20	L6_AA14_4P	AA14
21	GND		22	GND	
23	L6_T16_16P	T16	24	L6_W14_5P	W14
25	L6_U16_16N	U16	26	L6_Y14_5N	Y14
27	L6_W15_15P	W15	28	L6_AA15_3P	AA15
29	L6_W16_15N	W16	30	L6_AB15_3N	AB15
31	GND		32	GND	
33	L6_V15_13N	V15	34	L6_Y16_0P	Y16
35	L6_U15_13P	U15	36	L6_AA16_0N	AA16
37	/		38	L6_AB16_1P	AB16
39	L5_W19_GCLK	W19	40	L6_AB17_1N	AB17
41	GND		42	GND	
43	L5_P15_21P	P15	44	L5_R14_18N	R14
45	L5_R16_21N	R16	46	L5_P16_23P	P16
47	L5_N17_20P	N17	48	L5_R17_23N	R17
49	L5_P17_20N	P17	50	L5_V17_15P	V17
51	GND		52	GND	
53	L5_P19_4P	P19	54	L5_W17_15N	W17

55	L5_T19_4N	T19	**56**	L5_AA18_16P	AA18
57	L5_U17_17P	U17	**58**	L5_AB18_16N	AB18
59	L5_U18_17N	U18	**60**	L5_V18_13P	V18
61	L5_R18_19P	R18	**62**	L5_V19_13N	V19
63	L5_T18_19N	T18	**64**	L5_AA19_14P	AA19
65	L5_N13_22P	N13	**66**	L5_AB20_14N	AB20
67	L5_N14_22N	N14	**68**	L5_AA20_7P	AA20
69	L5_U20_10P	U20	**70**	L5_AA21_7N	AA21
71	L5_V20_10N	V20	**72**	L5_AB21_9P	AB21
73	L5_T21_3P	T21	**74**	L5_AB22_9N	AB22
75	L5_U21_3N	U21	**76**	L5_Y21_8P	Y21
77	L5_W21_6P	W21	**78**	L5_Y22_8N	Y22
79	L5_W22_6N	W22	**80**	GND	
81	NC		**82**	NC	

Expansion port J4 :

J4 Pins	Network Name	FPGA pins	J4 Pins	Network Name	FPGA Pins
1	5V		**2**	5V	
3			**4**		
5			**6**		
7			**8**		
9	GND		**10**	GND	
11	ADC_P	L10	**12**	NC	
13	ADC_N	M9	**14**	REST	Reset signal, low efficient
15	L6_AB11_6P	AB11	**16**	L6_W11_11P	W11
17	L6_AB12_6N	AB12	**18**	L6_W12_11N	W12
19	GND		**20**	GND	

21 *	R5_V9_20P	V9	**22**	L6_Y12_10N	Y12
23 *	R5_V8_20N	V8	**24**	L6_Y11_10P	Y11
25 *	R5_W9_23P	W9	**26**	L6_AA10_8P	AA10
27 *	R5_Y9_23N	Y9	**28**	L6_AA11_8N	AA11
29	GND		**30**	GND	
31*	R5_R3_2P	R3	**32**	L6_AA9_7P	AA9
33*	R5_R2_2N	R2	**34**	L6_AB10_7N	AB10
35*	R5_R4_12P	R4	**36**	L6_V10_9P	V10
37*	R5_T4_12N	T4	**38**	L6_W10_9N	W10
39	GND		**40**	GND	
41	L5_IO_P14	P14	**42**	NC	
43	L4_IO_K19	K19	**44**		
45	GND		**46**	GND	
47	NC		**48**	NC	
49	GND		**50**	GND	
51	NC		**52**	NC	
53	GND		**54**	GND	
55	NC		**56**	NC	
57			**58**		
59	GND		**60**	GND	
61	NC		**62**	NC	
63			**64**		
65	GND		**66**	GND	
67	NC		**68**	NC	
69	GND		**70**	GND	
71	NC		**72**	NC	
73			**74**		
75			**76**		
77			**78**		
79	GND		**80**	GND	

81	NC	**82**	NC

Note : IO marked with " * " is1.5V level standard, other IO is3.3V level standard; expansion port J5 :

J5 Pins	Network Name	FPGA pins	J5 Pins	Network Name	FPGA Pins
1	L3_C13_7P	C13	**2**	L3_F13_0P	F13
3	L3_B13_7N	B13	**4**	L3_F14_0N	F14
5	L3_C14_2P	C14	**6**	L3_E13_3P	E13
7	L3_C15_2N	C15	**8**	L3_E14_3N	E14
9	L3_D14_5P	D14	**10**	L3_E16_4P	E16
11	L3_D15_5N	D15	**12**	L3_D16_4N	D16
13	GND		**14**	GND	
15	MGT_TX0_P	D7	**16**	MGT_RX0_P	D9
17	MGT_TX0_N	C7	**18**	MGT_RX0_N	C9
19	GND		**20**	GND	
21	MGT_TX1_P	B6	**22**	MGT_RX1_P	B10
23	MGT_TX1_N	A6	**24**	MGT_RX1_N	A10
25	GND		**26**	GND	
27	MGT_CLK_P	F10	**28**	MGT_RX2_P	C5
29	MGT_CLK_N	E10	**30**	MGT_RX2_N	D5
31	GND		**32**	GND	
33	MGT_TX2_P	C11	**34**	MGT_RX3_P	A4
35	MGT_TX2_N	D11	**36**	MGT_RX3_N	B4
37	GND		**38**	GND	
39	MGT_TX3_P	A8	**40**	L3_F16_1P	F16
41	MGT_TX3_N	B8	**42**	L3_E17_1N	E17
43	GND		**44**	GND	
45	L3_A13_9P	A13	**46**	L3_D17_11P	D17
47	L3_A14_9N	A14	**48**	L3_C17_11N	C17

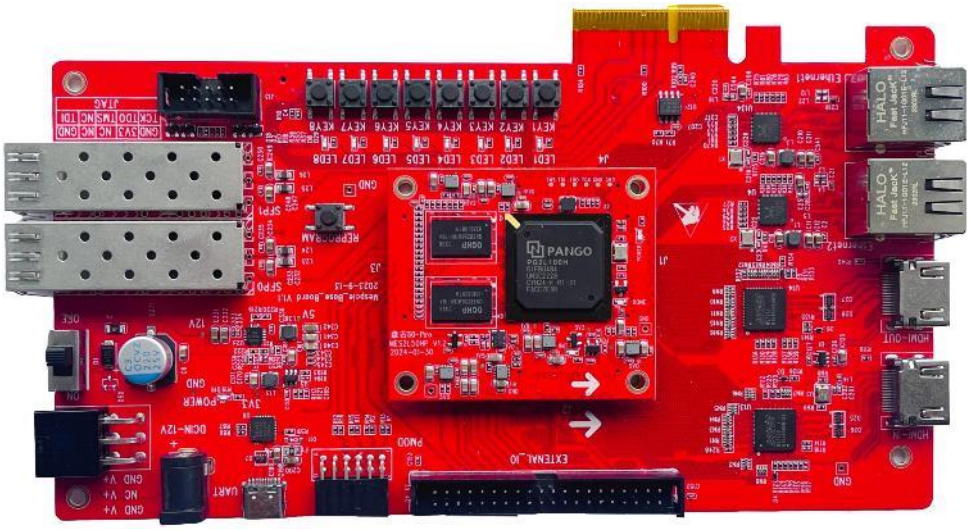
49	L3_A15_8P	A15	**50**	L3_F18_14P	F18
51	L3_A16_8N	A16	**52**	L3_E18_14N	E18
53	L3_B15_6P	B15	**54**	L3_B17_10	B17
55	L3_B16_6N	B16	**56**	L3_B18_10N	B18
57	L3_C18_12P	C18	**58**	L3_E19_13P	E19
59	L3_C19_12N	C19	**60**	L3_D19_13N	D19
61	GND		**62**	GND	
63	L3_A18_16P	A18	**64**	L3_D20_18P	D20
65	L3_A19_16N	A19	**66**	L3_C20_18N	C20
67	L3_B20_15P	B20	**68**	L3_E21_22P	E21
69	L3_A20_15N	A20	**70**	L3_D21_22N	D21
71	L3_B21_20P	B21	**72**	L3_C22_19P	C22
73	L3_A21_20N	A21	**74**	L3_B22_19N	B22
75	L3_D22_21N	D22	**76**	L3_E22_21P	E22
77	TDI		**78**	TCK	
79	TMS		**80**	TMS	
81	NC		**82**	NC	

3. Expansion baseboard

3.1 Introduction to the expansion baseboard

From the introduction of the previous development system, we know that the peripheral resources of the expansion baseboard are as follows:

- HDMI Input interface *1
- HDMI Output interface *1
- Optical fiber interface *2
- 10/100/1000M Ethernet interface *2
- PCIE X2 Interface *1
- JTAG Debug interface *1
- SD Card interface *1
- PMOD interface *1
- 40 pin IO Expansion port *1
- USB Serial port *1
- Buttons *8
- LEDs *8



3.2 External communication port

3.2.1 Network port

The MES2L484 series development board uses the Realtek RTL8211 PHY to implement a 10/100/1000 Ethernet port for network connection. The device supports 2.5V and 3.3V operating voltages. The PHY is connected to BANK L3 and connected to PG2L50H/PG2L100H/PG2L200H through the RGMII interface. The RJ-45 connector is HFJ11-1G01E-L12RL, which has integrated auto-winding magnetics to improve performance, quality, and reliability. The RJ-45 has two status indicator LEDs to indicate traffic and valid link status. Figure 3-1 below is a block diagram of the network port connection on the MES2L484 series development board.

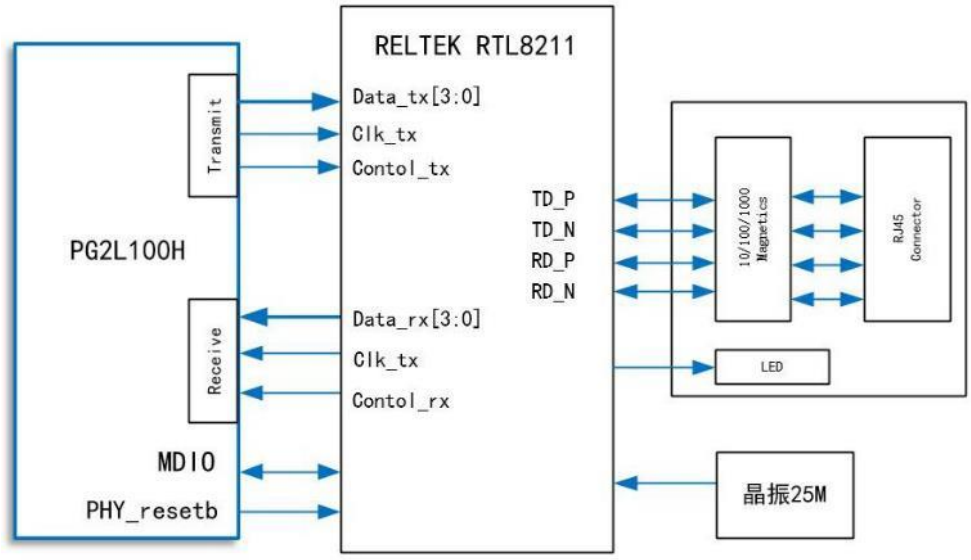


Figure 3-1 RTL8211 connection example

The following table shows the pin connections between network port 1 and PG2L484 series FPGA and RTL8211.

Table 3-1 PG2L484 Series connection RTL8211 Pin situation

Signal name	Description	FPGA Pin	RTL8211 Pin
RX_CLK	Receive clock line	C18	40
RX_CTRL	Receive control line	A14	37
RXD[3]	Receive data line 3	B16	38

RXD[2]	Receive data line 2	B15	39
RXD[1]	Receive data line 1	A16	41
RXD[0]	Receive data line 0	A15	42
TX_CLK	Send clock line	A18	47
TX_CTRL	Send control line	A21	2
TXD[3]	Send data line 3	B21	44
TXD[2]	Send data line 2	A20	45
TXD[1]	Send data line 1	B20	48
TXD[0]	Send data line 0	A19	1
MDC	Control bus clock	E22	5
MDIO	Control bus data	B22	4
RSTN	Reset control line, low effective	D22	29

The following table shows the pin connections between network port 2 and the PG2L484 series FPGA and RTL8211.

Table 3-2 PG2L484 series connected to RTL8211 pins

Signal name	Description	FPGA Pin	RTL8211 Pin
RX_CLK	Receive clock line	K18	40
RX_CTRL	Receive control line	G13	37
RXD[3]	Receive data line 3	G16	38
RXD[2]	Receive data line 2	J14	39
RXD[1]	Receive data line 1	H14	41

RXD[0]	Receive data line 0	H13	42
TX_CLK	Send clock line	F20	47
TX_CTRL	Send control line	F21	2
TXD[3]	Send data line 3	F15	44
TXD[2]	Send data line 2	G21	45
TXD[1]	Send data line 1	G22	48
TXD[0]	Send data line 0	F19	1
MDC	Control bus clock	G18	5
MDIO	Control bus data	G17	4
RSTN	Reset control line, low effective	G15	29

3.2.2 SFP Fiber Optic Interface

There are 2 fiber optic interfaces on the MES2L484 series development board. Users can use optical modules to connect to the fiber optic interfaces for fiber optic communication. The 2 fiber optic interfaces are connected to the 2 RX/TX of the HSST transceiver of the FPGA respectively. The TX signal and RX signal are connected to the FPGA and the optical module through DC isolation capacitors in differential signal mode. The data rate of each TX transmission and RX reception is up to 6.6Gb/s. The reference clock of the HSST transceiver is provided by the onboard 125M differential crystal oscillator.

The schematic diagram of the FPGA and fiber optic design is shown in the figure below:

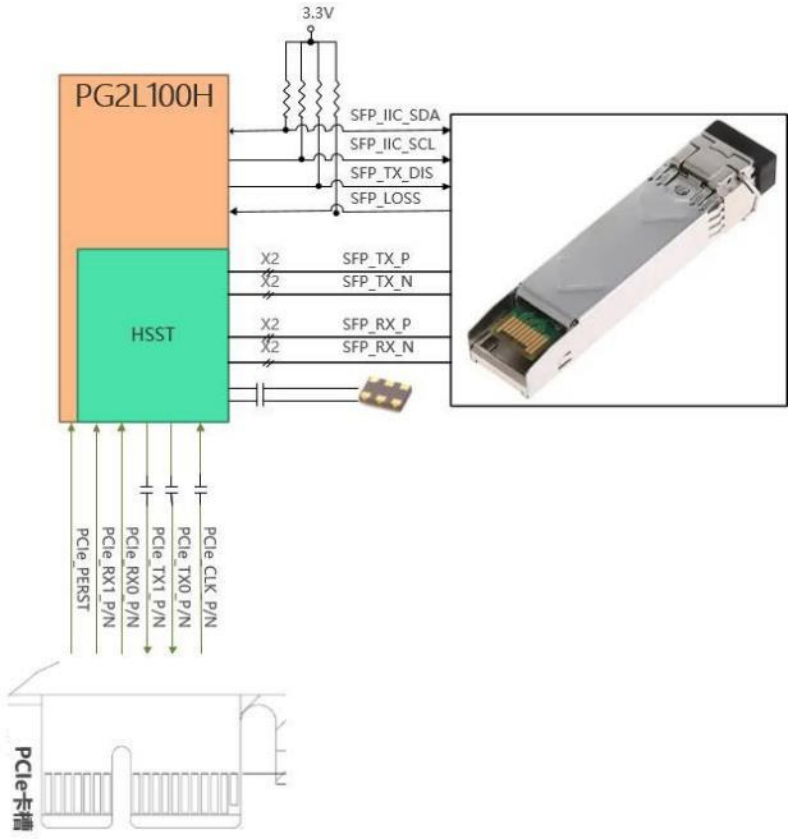


Figure 3-2 PG2L484 series HSST Functional connectivity diagram

The following table shows the pin connections between the PG2L484 series core board and the 2 SFP interfaces.

Table 3-3 PG2L484 Series Pin Assignment

Signal name	Description	FPGA Pin
SFP0_TXP	SFP0 Optical module data transmission P end	B6
SFP0_TXN	SFP0 Optical module data transmission N end	A6
SFP0_RXP	SFP0 Optical module data reception P end	B10
SFP0_RXN	SFP0 Optical module data reception N end	A10
SFP0_LOS	SFP0 optical module receives Loss signal. High means no optical signal is received.	E19

SFP0_SCl	SFP0 Optical Module I2C Communication clock	B18
SFP0_SDA	SFP0 Optical Module I2C Communication data	B17
SFP0_TX_DISABLE	SFP0 Optical module light emission is prohibited, high effective	E18
SFP1_TXP	SFP1 Optical module data transmission P end	D7
SFP1_TXN	SFP1 Optical module data transmission N end	C7
SFP1_RXP	SFP1 Optical module data reception P end	D9
SFP1_RXN	SFP1 Optical module data reception N end	C9
SFP1_LOS	SFP1 optical module receives Loss signal. High means no optical signal is received.	E21
SFP1_SCl	SFP1 Optical Module I2C Communication clock	C20
SFP1_SDA	SFP1 Optical Module I2C Communication data	D20
SFP1_TX_DISABLE	SFP1 Optical module light emission is prohibited, high effective	D19

3.2.3 PCIe X2 interface

The expansion baseboard of the MES2L484 series development board provides an industrial-grade high-speed data transmission PCIex2 interface. The dimensions of the PCIE card meet the electrical specifications of the standard PCIe card and can be used directly on the x4 PCIe slot of an ordinary PC.

The transmit and receive signals of the PCIe interface are directly connected to the HSST transceiver of the FPGA. The TX and RX signals of the two channels are connected to the FPGA in a differential signal mode. The single-channel communication rate can be as high as 5G bit bandwidth. The reference clock of PCIe is provided to the development board by the PCIe slot of the PC, and the reference clock frequency is 100Mhz.

The design diagram of the PCIe interface of the development board is shown in the optical fiber connection reference diagram above, where the TX transmit signal and the reference clock CLK signal are connected in AC coupling mode.

The pin connection between the PG2L484 series FPGA and the PCIe card slot is shown in the following table.

Table 3-4 PG2L484 Series Pin Assignment

Signal name	Description	FPGA Pin
PCIE_TX0P	PCIe aisle 0 Data transmission P end	B4
PCIE_TX0N	PCIe aisle 0 Data transmission N end	A4
PCIE_TX1P	PCIe aisle 1 Data transmission P end	D5
PCIE_TX1N	PCIe aisle 1 Data transmission N end	C5
PCIE_RX0P	PCIe aisle 0 Data Reception P end	B8
PCIE_RX0N	PCIe aisle 0 Data Reception N end	A8
PCIE_RX1P	PCIe aisle 1 Data Reception P end	D11
PCIE_RX1N	PCIe aisle 1 Data Reception N end	C11
PCIE_refclk_P	PCIe Reference clock P end	F10
PCIE_refclk_N	PCIe Reference clock N end	E10
PCIE_PERST	PCIe Reset pin	C22
PCIE_WAKE	PCIe Wake-up pin	D21

3.2.4 Serial Port

The MES2L484 series expansion board integrates a USB-to-serial port module. The USB-UART chip used is CP2102. The USB interface uses a USB Type C interface. You can use a USB Type C cable to connect it to the USB port of the PC for serial data communication.

The schematic diagram of the USB Uart circuit design is shown below:

Figure 3-3 USB-UART Block Diagram

Table 3-5 UART Pinout

Signal name	Description	FPGA Pin
UART0_TX	Uart Data Output	K19
UART0_RX	Uart data input	P14

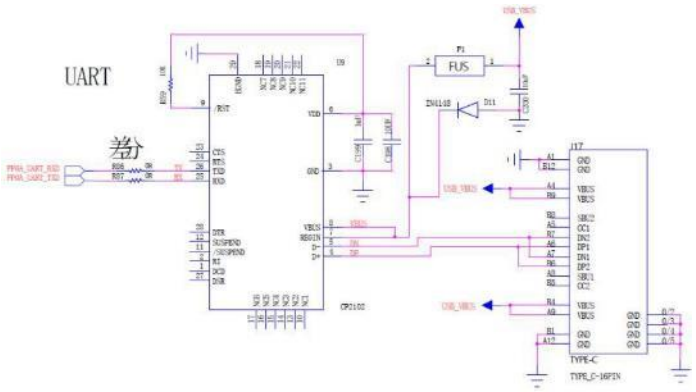


Figure 3-4 USB-UART Circuit

3.2.5 JTAG

The JTAG interface on the MES2L484 series development board is used to download FPGA programs or solidify programs to FLASH. In order to reduce the damage to the FPGA chip caused by hot plugging, a protection diode is added to the JTAG signal position in the design to ensure that the signal voltage is within the range accepted by the FPGA to avoid damage to the FPGA.

Reminder: Avoid hot plugging when the power is on.

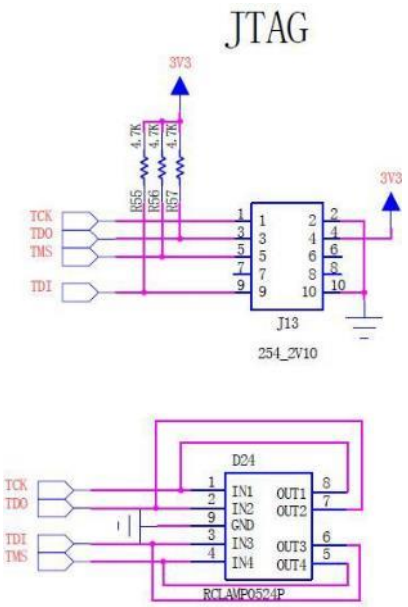


Figure 3-5 JTAG Connector Schematic Diagram

3.3 HDMI

3.3.1 HDMI input interface

The HDMI input interface is implemented using the MS7200 HMDI receiver chip from China's Hongjing Micro, which is compatible with HDMI1.4b and the 3D transmission format of standard video under HDMI 1.4b. The highest resolution supported is up to 4K@30Hz, and the highest sampling rate is 300MHz; MS7200 supports color space conversion between YUV and RGB, and the digital interface supports YUV and RGB format output;

MS7200 supports high-definition audio transmission via IIS bus or SPDIF, and also supports high-bit audio (HBR) audio. In HBR mode, the audio sampling rate is up to 768KHz. Among them, the IIC configuration interface of MS7200 is connected to the IO of FPGA. The MS7200 is initialized and controlled by programming of FPGA. The SA pin of MS7200 is pulled down to the ground on the MES2L484 series P development board, so the ID address of IIC is 0x56;

The hardware connection of HDMI input interface is shown in the figure below.

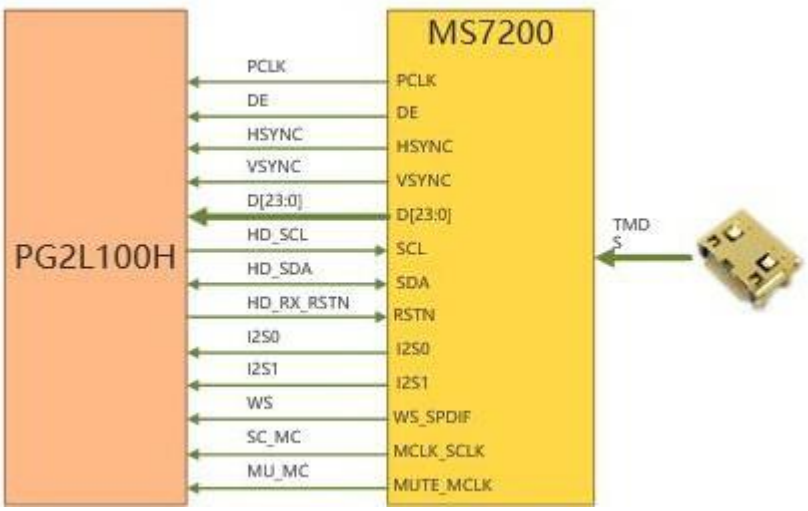


Figure 3-6 HDMI Receiver Connection diagram

Please see the following table for specific pin assignments:

Table 3-6 HDMI pin assignment

Signal name	Description	FPGA Pin
HD_RX_PCLK	HDMI Display image pixel clock	W19
HD_RX_VS	HDMI Display image frame synchronization signal	P15
HD_RX_HS	HDMI Display image line synchronization signal	R16
HD_RX_DE	HDMI Display image valid pixel enable signal	R14
HD_RX_D0	HDMI Display image pixel data bit [0]	P16
HD_RX_D1	HDMI Display image pixel data bit [1]	R17
HD_RX_D2	HDMI Display image pixel data bit [2]	V17
HD_RX_D3	HDMI Display image pixel data bits [3]	W17
HD_RX_D4	HDMI Display image pixel data bits [4]	AA18
HD_RX_D5	HDMI Display image pixel data bit [5]	AB18
HD_RX_D6	HDMI Display image pixel data bit [6]	V18
HD_RX_D7	HDMI Display image pixel data bits [7]	V19
HD_RX_D8	HDMI Display image pixel data bit [8]	AA19

HD_RX_D9	HDMI display image pixel data bit[9]	AB20
HD_RX_D10	HDMI display image pixel data bit[10]	AA20
HD_RX_D11	HDMI display image pixel data bit [11]	AA21
HD_RX_D12	HDMI display image pixel data bit [12]	V20
HD_RX_D13	HDMI display image pixel data bit [13]	U20
HD_RX_D14	HDMI display image pixel data bit [14]	N14
HD_RX_D15	HDMI display image pixel data bit [15]	N13
HD_RX_D16	HDMI display image pixel data bit [16]	T18
HD_RX_D17	HDMI display image pixel data bit [17]	R18
HD_RX_D18	HDMI display image pixel data bit [18]	U18
HD_RX_D19	HDMI display image pixel data bit [19]	U17
HD_RX_D20	HDMI display image pixel data bit [20]	T19
HD_RX_D21	HDMI display image pixel data bit [21]	P19
HD_RX_D22	HDMI display image pixel data bit [22]	P17
HD_RX_D23	HDMI display image pixel data bit [23]	N17
HD_SCL	MS7200 control channel IIC clock signal	Y21
HD_SDA	MS7200 control channel IIC data signal	Y22
HD_RX_SC_MC	MS7200 audio channel I2S serial clock signal	W21
HD_RX_MU_MC	MS7200 audio channel I2S master clock signal or mute signal	J16
HD_RX_I2S1	MS7200 Audio Channel I2S Data Channel 1	U21
HD_RX_I2S0	MS7200 Audio Channel I2S Data Channel 0	T21
HD_RX_WS_SP	MS7200 Audio Channel I2S Bit Clock	W22
HD_RX_RSTN	MS7200 hardware reset signal, low level is effective	AB22
HD_RX_INT	MS7200 output interrupt signal	AB21

3.3.2 HDMI Output Interface

The HDMI output interface is realized by using the MS7210 HMDI transmitter chip of the domestic Hongjing Micro Company, which is compatible with HDMI1.4b and the 3D transmission format of standard video under HDMI 1.4b. It has a built-in programmable EDID cache, supports a maximum resolution of up to 4K@30Hz, and a maximum sampling rate of 300MHz; MS7210 supports color space conversion between YUV and RGB, and the digital interface supports YUV and RGB format input; the IIS interface of MS7210 supports the transmission of high-definition audio, and also supports high-bit audio (HBR) audio. In HBR mode, the audio sampling rate is up to 768KHz.

Among them, the IIC configuration interface of MS7210 is connected to the IO of FPGA. The MS7210 is initialized and controlled by programming of FPGA. The SA pin of MS7210 is pulled up to the power supply voltage on the MES2L484 series P development board, so the ID address of IIC is 0xB2;

The hardware connection of HDMI output interface is shown in the figure below.

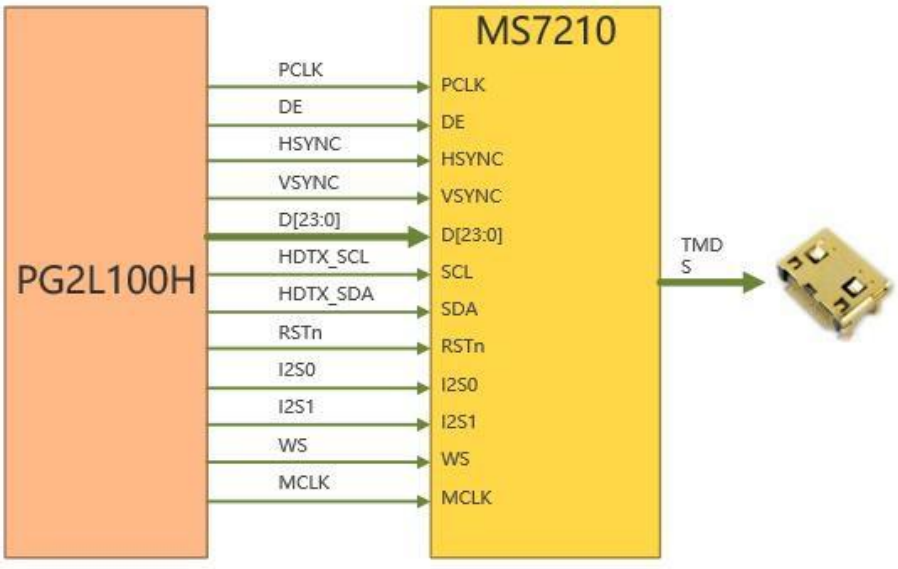


Figure 3-7 HDMI Transmit Connection diagram

Please see the following table for specific pin assignments :

Table 3-7 HDMI Pin Assignment

Signal name	Description	FPGA Pin
HD_TX_PCLK	HDMI Display image pixel clock	L20
HD_TX_VS	HDMI Display image frame synchronization signal	M17
HD_TX_HS	HDMI Display image line synchronization signal	M18
HD_TX_DE	HDMI Display image valid pixel enable signal	L18
HD_TX_D0	HDMI Display image pixel data bit [0]	M15
HD_TX_D1	HDMI Display image pixel data bit [1]	M16
HD_TX_D2	HDMI Display image pixel data bit [2]	L14
HD_TX_D3	HDMI Display image pixel data bits [3]	L15
HD_TX_D4	HDMI Display image pixel data bits [4]	M13
HD_TX_D5	HDMI Display image pixel data bit [5]	L13
HD_TX_D6	HDMI Display image pixel data bit [6]	K21
HD_TX_D7	HDMI Display image pixel data bits [7]	K22
HD_TX_D8	HDMI Display image pixel data bit [8]	L19
HD_TX_D9	HDMI Display image pixel data bit [9]	K17
HD_TX_D10	HDMI Display image pixel data bit [10]	J17
HD_TX_D11	HDMI Display image pixel data bit [11]	L16
HD_TX_D12	HDMI Display image pixel data bit [12]	K16
HD_TX_D13	HDMI Display image pixel data bits [13]	K13
HD_TX_D14	HDMI Display image pixel data bits [14]	K14
HD_TX_D15	HDMI Display image pixel data bit [15]	J22
HD_TX_D16	HDMI Display image pixel data bits [16]	H22
HD_TX_D17	HDMI Display image pixel data bits [17]	J20
HD_TX_D18	HDMI Display image pixel data bit [18]	J21

HD_TX_D19	HDMI Display image pixel data bits [19]	H17
HD_TX_D20	HDMI Display image pixel data bit [20]	H18
HD_TX_D21	HDMI Display image pixel data bit [21]	J15
HD_TX_D22	HDMI Display image pixel data bit [22]	H15
HD_TX_D23	HDMI Display image pixel data bit [23]	H20
HDMI_TX_SCL	MS7210 Control Channel IIC The clock signal	M21
HDMI_TX_SDA	MS7210 Control Channel IIC Data signal	L21
HD_TX_SC_MC	MS7210 Audio Channels I2S The clock signal	N19
HD_TX_I2S1	MS7210 Audio Channels I2S Data Channel 1	N22
HD_TX_I2S0	MS7210 Audio Channels I2S Data Channel 0	M20
HD_TX_WS	MS7210 Audio Channels I2S The bit clock	N18
HD_TX_RSTN	MS7210 Hardware reset signal, low level is effective	AB22
HD_TX_INT	MS7210 Output interrupt	N20

3.4 Buttons / LEDs

3.4.1 Buttons

The MES2L484 series expansion base provides 8 user buttons (K1~8); 1 reload button, which is connected to the RSTN pin of PG2L50H/PG2L100H/PG2L200H through a delay reset chip; the 8 user buttons are connected to the common IO of PG2L50H/PG2L100H/PG2L200H, the button is valid at low level, but when the button is pressed, the input voltage on the IO is low; when the button is not pressed, the input voltage on the IO is high;

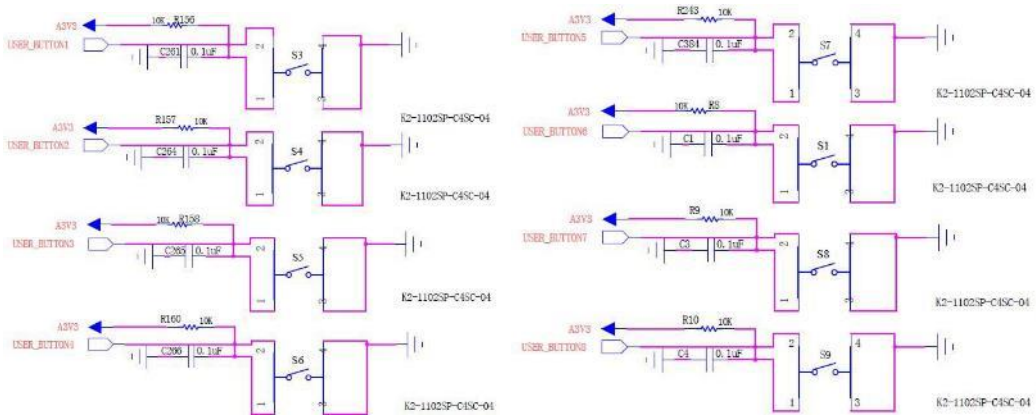


Figure 3-8 User button circuit diagram

The specific pin assignments are as follows ;

Table 3-8 Button pin assignment

Signal	FPGA Pin
REST	Reload firmware button
KEY1	Y19
KEY2	W20
KEY3	T20
KEY4	V22
KEY5	P20
KEY6	N15
KEY7	J19
KEY8	H19

3.4.2 LEDs

The MES2L484 series development board has 11 green LED lights, one of which is the power indicator (POWER); two are FPGA operation status indicators: INIT and DONE; and eight are user LED lights (LED1 to 8). Connected to the IO of BANK L3 of PG2L50H/PG2L100H/PG2L200H, the corresponding LED lights light up when the FPGA outputs a high level. The LED function circuit diagram on the board is shown in the figure below:

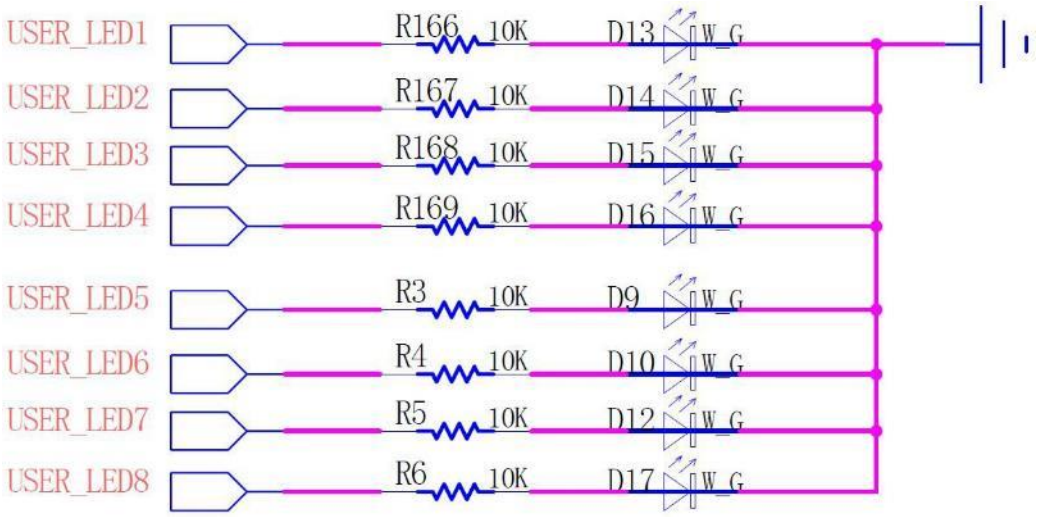


Figure 3-9 LEDs connection circuit diagram

Please refer to the following table for specific pin assignments :

Table 3-9 led lamp

Signal	FPGA Pin
LED1	F13
LED2	F14
LED3	E13
LED4	E14
LED5	E16
LED6	D16
LED7	F16
LED8	E17

3.5 Storage Interface

3.5.1 EEPROM

The MES2L484 series development board has an EEPROM onboard, model 24LC02, capacity: 2Kbit (1*256*8bit), and an onboard EEPROM needs to use the IIC bus for read and write operations, so it can be used to learn the communication method of the IIC bus. The I2C signal of the EEPROM is connected to the IO port of the FPGA. The following figure is a schematic diagram of the design of the EEPROM; it consists of 256-byte blocks and communicates through the IIC bus.

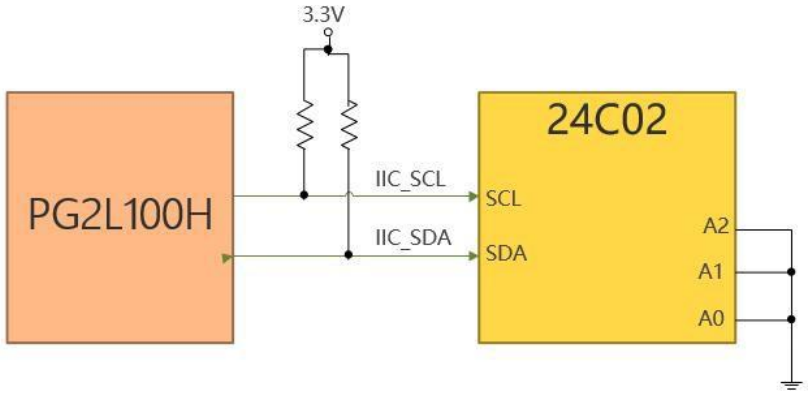


Figure 3-10 EEPROM Design Schematic

The EEPROM pin assignments are as follows:

Table 3-10 EEPROM Pinout

Signal	Description	FPGA Pin
IIC_SCL	EEPROM clock	C19
IIC_SDA	EEPROM data	A13

3.5.2 SD CARD

SD card is a common storage device. The SD card expanded by the MES2L484 series development board supports SPI mode and SD mode. The SD card used is a MicroSD card. The schematic diagram is shown in Figure 3-11 below. The SD card signal level is 3.3V.

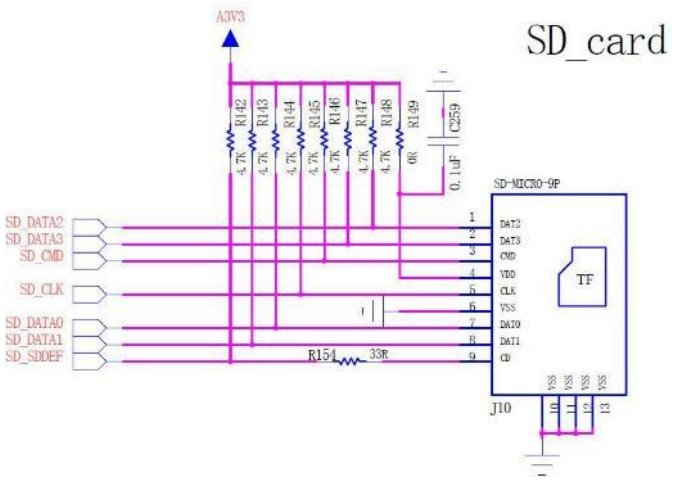


Figure 3-11 SDCARD Circuit

Table 3-11 SDCARD Pinout Example

Signal	Description	FPGA Pin	SD Card Pin
CLK	Clock	C14	5
CMD	Command Serial Line	C15	3
DATA[0:3]	Data bus	D0: B13	7
		D1: C13	8
		D2: D15	1
		D3: D14	2
DETECT	Card recognition	D17	9

3.6 Expansion port

3.6.1 40pin Expansion port

The expansion board reserves a 40-pin expansion port J16 with a standard spacing of 2.54mm, which is used to connect various modules or various peripheral circuits. The expansion port has 40 signals, including 1 5V power supply, 2 3.3V power supplies, 3 grounds, and 34 IO ports. Do not connect the expansion port IO directly to a 5V device to avoid burning the FPGA. If you need to connect a 5V device, you need to connect a level conversion chip.

When using 40PIN expansion IO to transmit differential signals, please note that the left side of the MES2L484 series baseboard schematic diagram is N-terminal except EX_IO_11P and EX_IO_7P, and the right side is P-terminal except EX_IO_11N and EX_IO_7N.

The MES2L484-50AG development board does not support 40pin expansion ports.

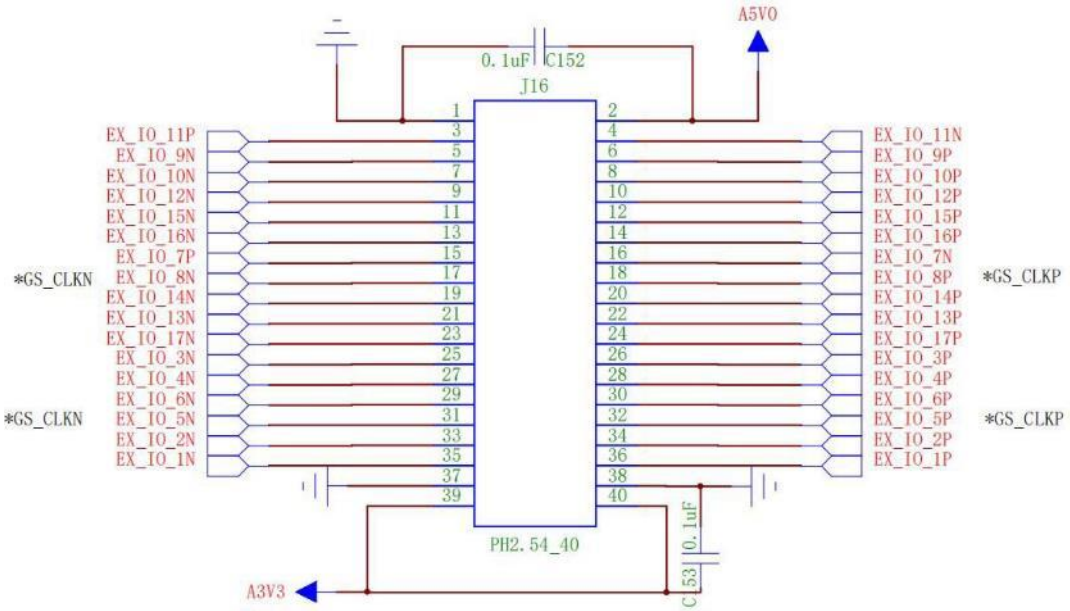


Figure 3-12 40pin Extensions IO Schematic

Table 3-12 40pin Extensions IO

Pin #	Network Name	FPGA Pins		Pin #	Network Name	FPGA Pins
1	GND	\		2	5V0	\
3	EX_IO_11P	AB16		4	EX_IO_11N	AB17
5	EX_IO_9N	AB15		6	EX_IO_9P	AA15
7	EX_IO_10N	W16		8	EX_IO_10P	W15
9	EX_IO_12N	Y14		10	EX_IO_12P	W14
11	EX_IO_15N	U16		12	EX_IO_15P	T16
13	EX_IO_16N	AA14		14	EX_IO_16P	Y13
15	EX_IO_7P	Y16		16	EX_IO_7N	AA16

17	EX_IO_8N	V15		18	EX_IO_8P	U15
19	EX_IO_14N	T15		20	EX_IO_14P	T14
21	EX_IO_13N	AB13		22	EX_IO_13P	AA13
23	EX_IO_17N	V14		24	EX_IO_17P	V13
25	EX_IO_3N	W10		26	EX_IO_3P	V10
27	EX_IO_4N	AB10		28	EX_IO_4P	AA9
29	EX_IO_6N	AA11		30	EX_IO_6P	AA10
31	EX_IO_5N	Y12		32	EX_IO_5P	Y11
33	EX_IO_2N	W12		34	EX_IO_2P	W11
35	EX_IO_1N	AB12		36	EX_IO_1P	AB11
37	GND	\		38	GND	\
39	A3V3	\		40	A3V3	\

3.6.2 PMOD Expansion port

The MES2L484 series expansion baseboard has a 12-pin 2.54mm pitch PMOD interface (J11) reserved for connecting the FPGA to external modules or circuits. Please note that the signals of the connected external devices and circuits require a 3.3V level standard. The schematic diagram of the PMOD connector is shown below:

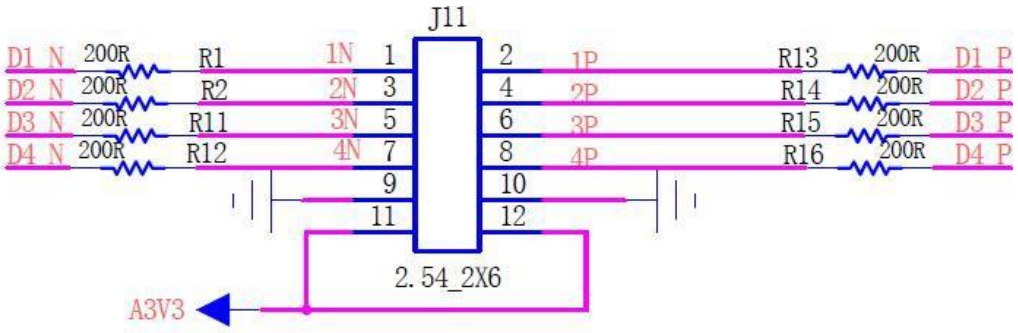


Figure 3-13 PMOD Socket connection schematic diagram

Table 3-13 PMOD Pin Assignment

Pin #	Network Name	FPGA Pins		Pin #	Network Name	FPGA Pins
1	D1_N	V8		2	D1_P	V9
3	D2_N	Y9		4	D2_P	W9
5	D3_N	R2		6	D3_P	R3
7	D4_N	T4		8	D4_P	R4
9	GND	\		10	GND	\
11	A3V3	\		12	A3V3	\

3.7 Power supply

The power input voltage of the development board is +12V. Please use the power supply that comes with the development board. Do not use power supplies of other specifications to avoid damaging the development board. The expansion board uses a DC/DC power chip SGM61163 to convert the +12V voltage into a +5V power supply with a maximum output current of 6A; another DC/DC power chip MT2492 is used to convert +5V into a +3.3V power supply with a maximum output current of 2A for use by the peripheral interface; the +5V power supply on the expansion board supplies power to the core board through the inter-board connector. The power supply design on the expansion board is shown in the figure below:

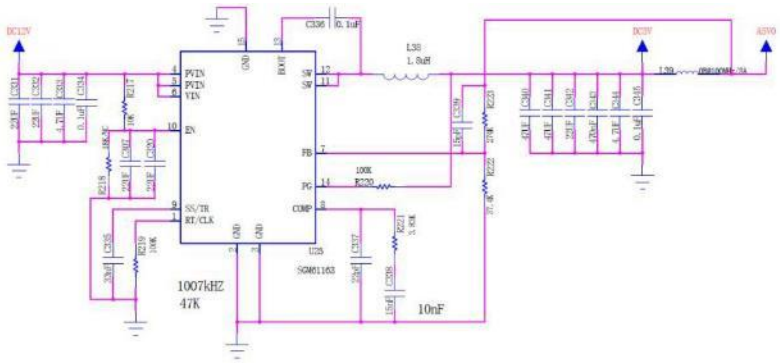


Figure 3-14 12V to 5V schematics

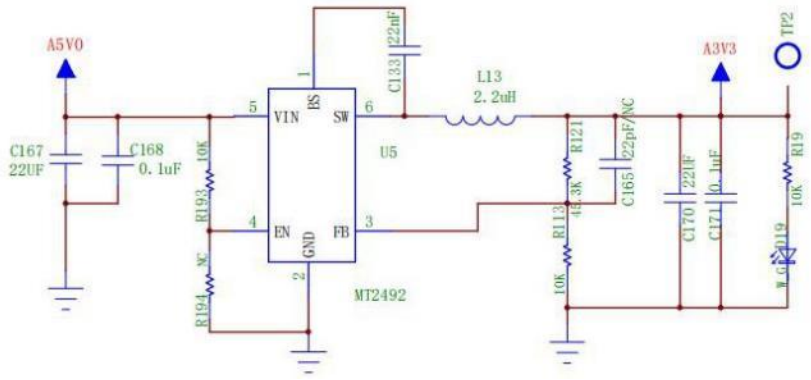


Figure 3-15 5V to 3.3V schematic

3.8 Dimensional structure diagram

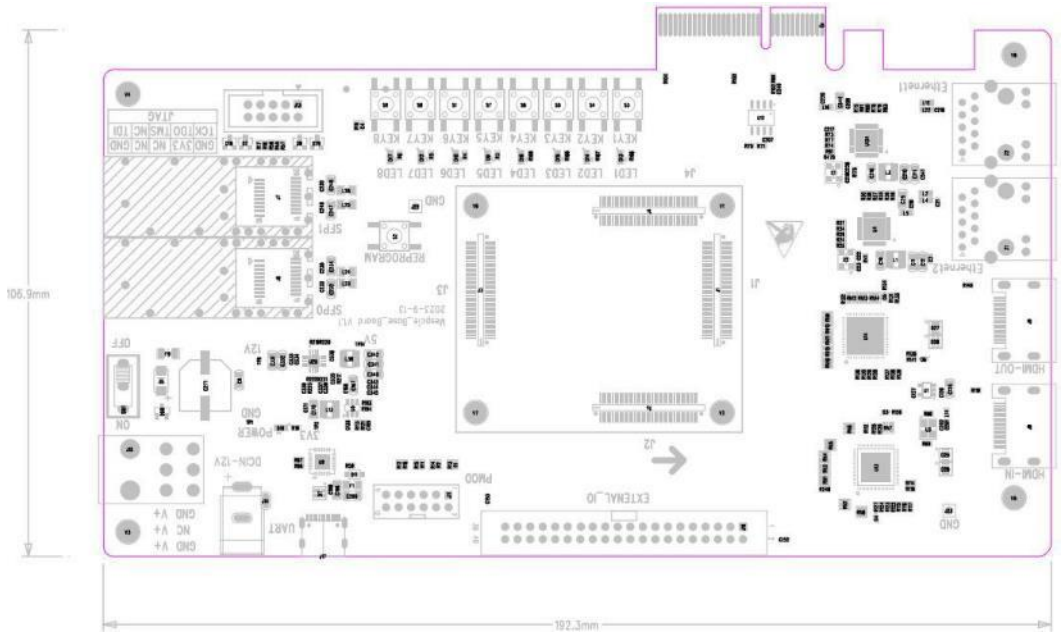


Figure 3-16 Expansion baseboard size diagram