Product Specification

PART NUMBER # REV: FLC-070QMMG000SA1#00

DESCRIPTION: TFT 7"W, 800(H)*1280(V), MIPI, Full View, 450CD

(   )   Preliminary Specification

(V)   Approved Specification

Customer Name:	
Signature:	**Date:**

PREPARED BY	REVIEWED BY
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Revision History

Version	Date	Page	Description	Note
V1.0	2021/03/19		1st initial	

Table of Content

1. GENERAL DESCRIPTION

1.1 Description

7 inch is a Color Active Matrix Liquid Crystal Display Module composed of a TFT LCD panel and LED backlight system. The screen format is intended to support the 800 x 1280 screen.

1.2 Product Summary

The following items are summary on the table under Ta=25 °C condition:

No.	Item	Specification	Unit
1	Display Size	7	Inch
2	Pixel Number	800 (H) x 3(RGB)x 1280 (V)	Pixels
3	Outline Dimension	103.46(W) x 162.26(H) x 2.45(Typ.) 4.5(D)(Max. PCB zone)	mm
4	Active Area	94.2 (W) x 150.72 (H)	mm
5	Pixel Pitch	0.11775 (H) x 0.11775 (V)	mm
6	Pixel Arrangement	RGB Vertical stripe	- -
7	Display Mode	IPS, Normally Black	- -
8	Electrical Interface	4 wire MIPI	- -
9	Surface Treatment	Anti-Glare	
10	Brightness	450 (Typ.)	cd/m2
11	Contrast Ratio	800 (Typ.)	--
12	Power Consumption	Backlight: 1.5 (Max)	W

2. ABSOLUTE MAXIMUM RATING

2.1 Electrical Absolute Rating

Item	Symbol	Values			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	VCI	-0.3	-	3.6	V	GND=0
Logic Supply Voltage	VCC	-0.3	-	VCC+0.3	V	

2.2 Backlight Converter

Item	Symbol	Values			Unit	Note
		Min	Typ	Max		
Current of Backlight Unit	Ib	-	80	-	mA	
Voltage of Backlight Unit	Vb	-	15	16.5	V	

Note: Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is loaded.

2.3 Environment Absolute Rating

Item	Symbol	Values			Unit	Note
		Min	Typ	Max.		
Operating Temperature	Top	-20	-	+70	°C	
Storage Temperature	Tstg	-30	-	+80	°C	

3. ELECTRICAL CHARACTERISTICS

3.1 LCD Electrical Specification

Parameter		Min.	Typ.	Max.	Unit	Note
Power supply voltage	VDDIN	3.0	3.3	3.6	V	
	Ivddin	-	NA	-	mA	
Input voltage 'H' Level	VIH	0.7VDD	-	VCI	V	
Input voltage 'L' Level	VIL	0	-	0.3VDD	V	

3.2 Backlight Unit

The backlight system is an edge-lighting type with 20 LED. The characteristics of the LED are shown in the following tables.:

Parameter	Symbol	Min.	Type	Max.	Unit.	Note
LED Current	IL	-	80	-	mA	(2)
LED Voltage	VL	-	15	16.5	V	
LED Life Time	Hr	50,000	-	-	Hrs	(1) (2)

Note 1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25 ±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=80mA. The LED lifetime could be decreased if operating IL is larger than 80mA. The constant current driving method is suggested.

3.3 AC Characteristics

3.3.1 DSI layer definitions

According to DSI transmitter and receiver interface to understand simple interface block diagram. Then under diagram is internal block for DSI which include four types: PHY Layer, Lane Management Layer, Low level protocol and Application Layer.

The PHY Layer specifies the characteristics of transmission medium and electrical parameters for signaling the timing relationship between clock and Data Lanes.

The Lane Management Layer specifies DSI is Lane-scalable for increased performance. The data signals maybe transmission through one or more channel depending on the bandwidth requirements of the application.

The protocol Layer specifies at the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets.

The Application Layer describes higher-level encoding and interpretation of data contained in the data stream. The DSI specification describes the mapping of pixel values, commands and command's parameters to bytes in the packet assembly.
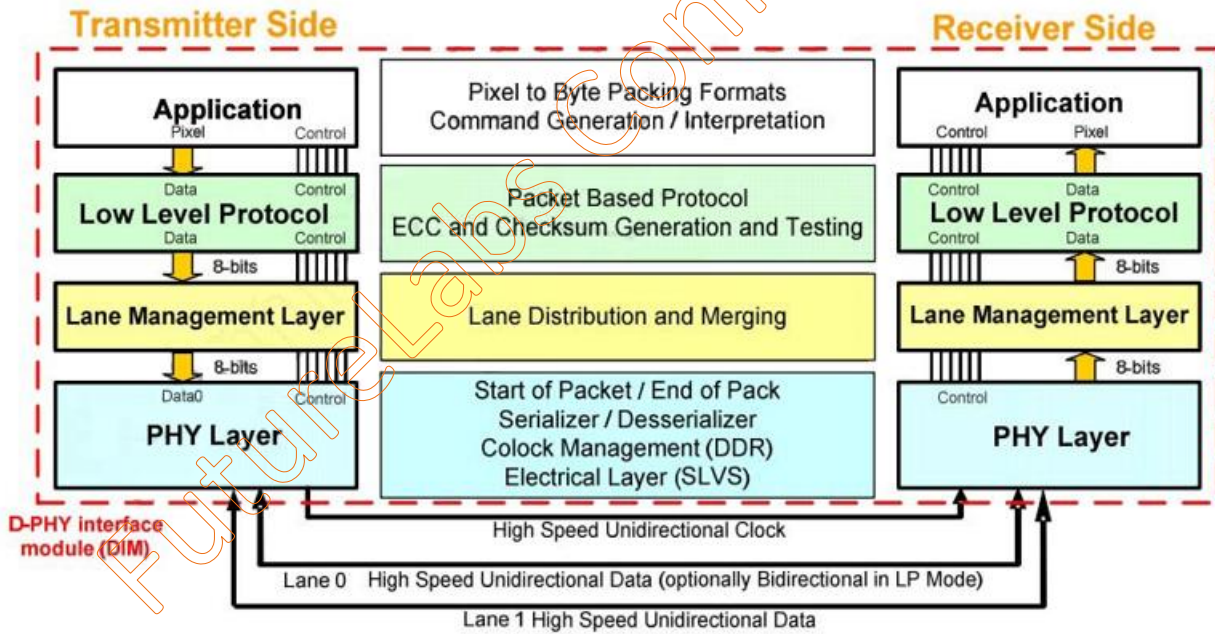
DSI Layer

The state code of HS and LP Lane pair are defined as below:

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	Note 1	Note 1
HS-1	HS High	HS Low	Differential-1	Note 1	Note 1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
Lp-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
Lp-11	LP High	LP High	N/A	Stop	Note 2

Note 1: During High-Speed Transmission the Low-Power Receivers observe LP-00 on the Lines.

Note 2: If LP-11 occurs during Escape mode the Lane returns to Stop state (Control Mode LP-11)

3.3.2 Clock lane mode

Figure as below shows the state diagram for Clock Lane Mode. The Clock Lane has three different power modes: Low Power Stop State, Ultra Low Power State (ULPS) and High Speed clock transmission.
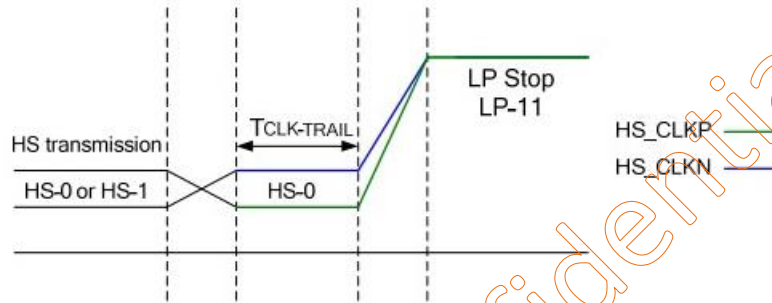

Clock Lane Mode state diagram
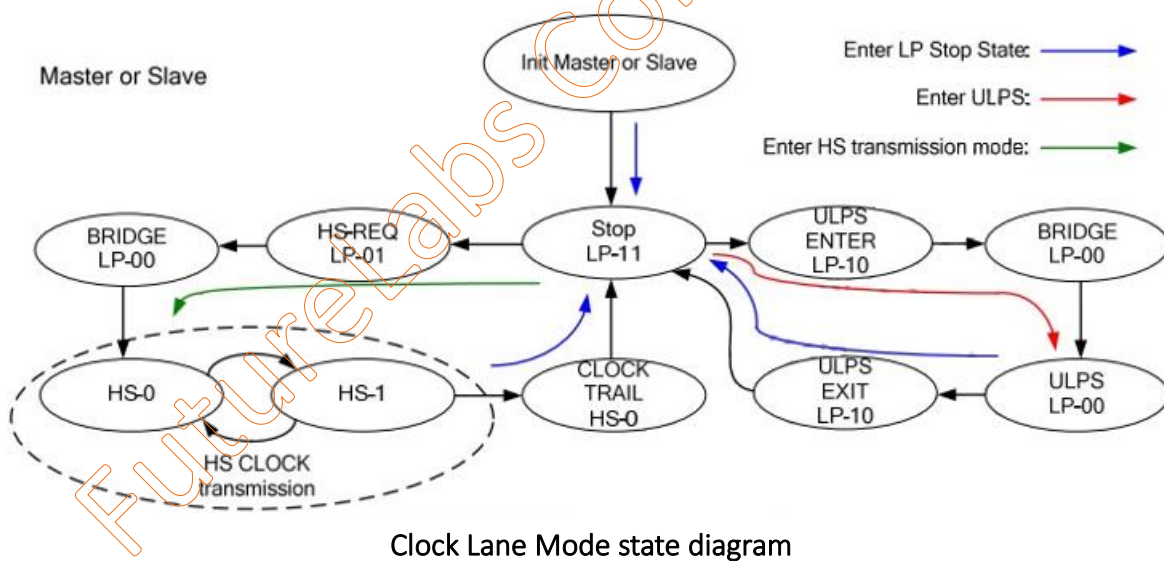
Clock Lane can be driven LP-11 to enter Low Power Stop State. There are three ways to enter Lower Power Stop State:

A. After Initial State (HW reset, SW reset, Power on sequence).

B. Leaving ULPS: ULPS LP-00→LP-10→Low Power Stop State LP-11.
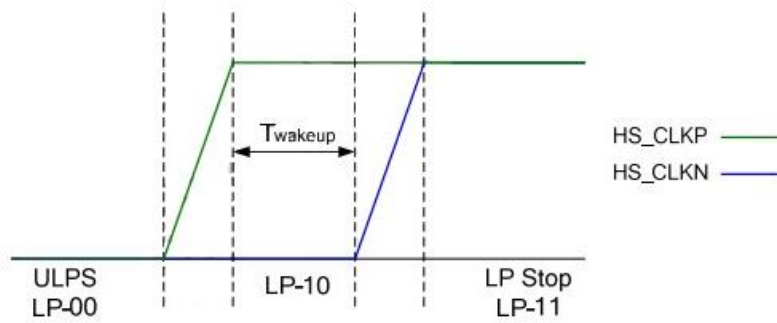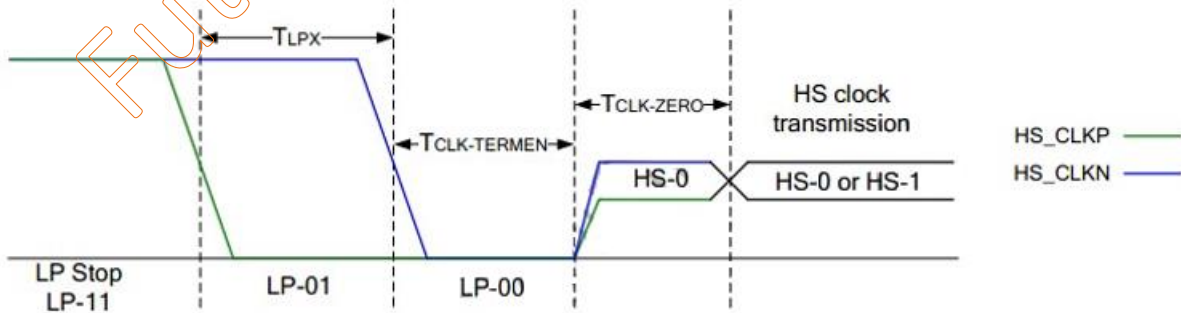
C. Leaving HS Clock transmission mode: HS mode (HS-0 or HS-1) →HS-0→Low Power Stop State LP-11.

Clock Lane can be driven LP-00 to enter Ultra Low Power State from Low Power Stop State. The flow is Low Power Stop State LP-11→LP-10→ULPS LP-00
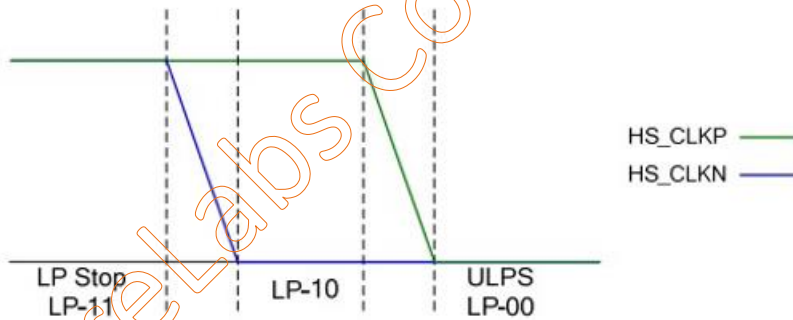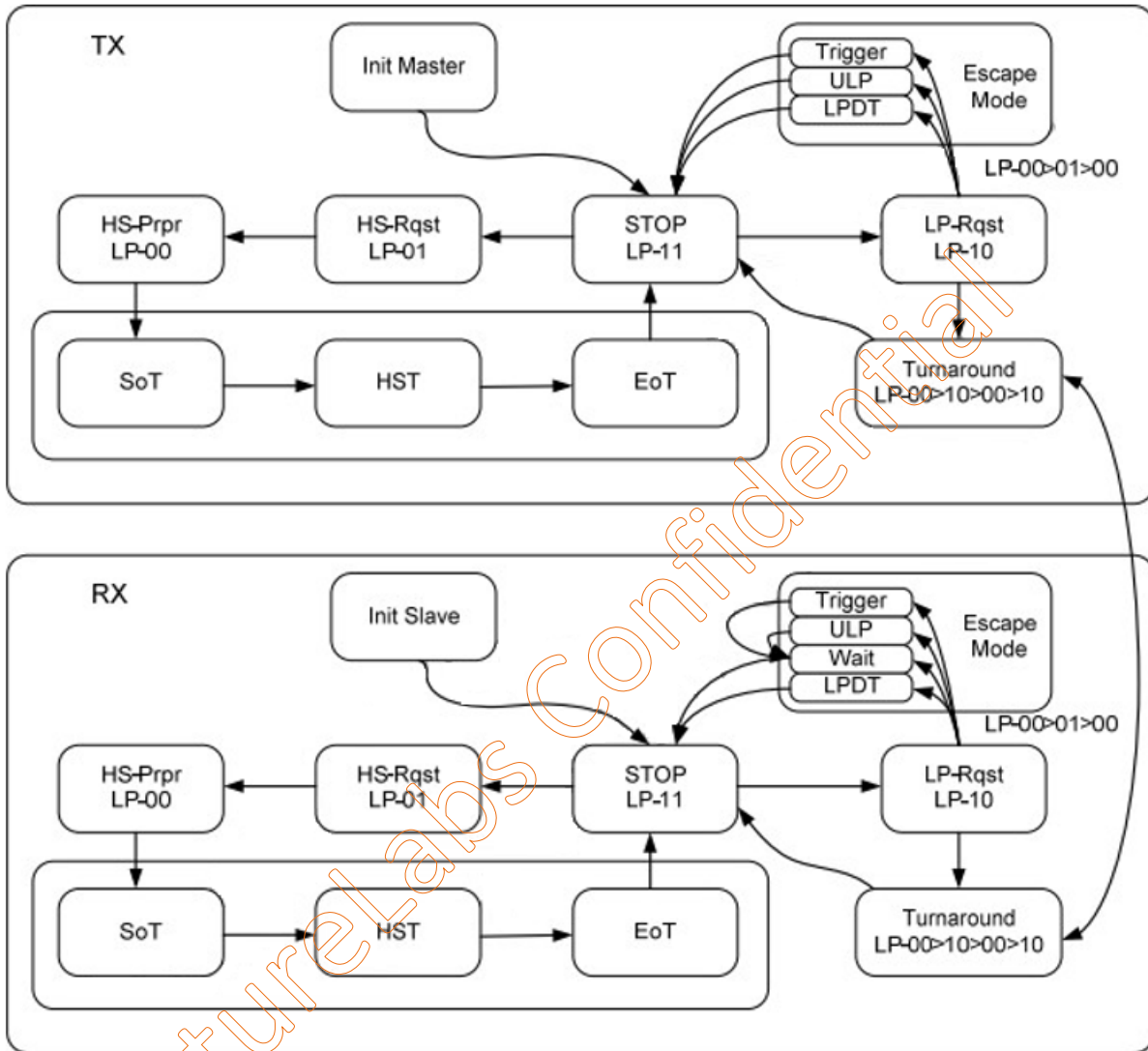

Clock Lane can be High Speed Clock transmission State from Low Power Stop State. The flow is Low Power Stop State LP-11→LP-01→LP-00→HS-0→HS-0/1.

3.3.3 Data Lane Mode

Figure as below shows the operational flow diagram for Data Lane Mode. There are three operating modes in Data Lane: Escape mode, High-Speed transmission mode and Turn around.


Data lane mode state diagram

3.3.4 Escape Mode

Data Lane 0 is used in Escape Mode when data lane in LP mode. Data Lane shall enter Escape mode via LP-110, LP-100, LP-000, LP-010, Lp-00 and exit Escape mode via LP-100, LP-11.
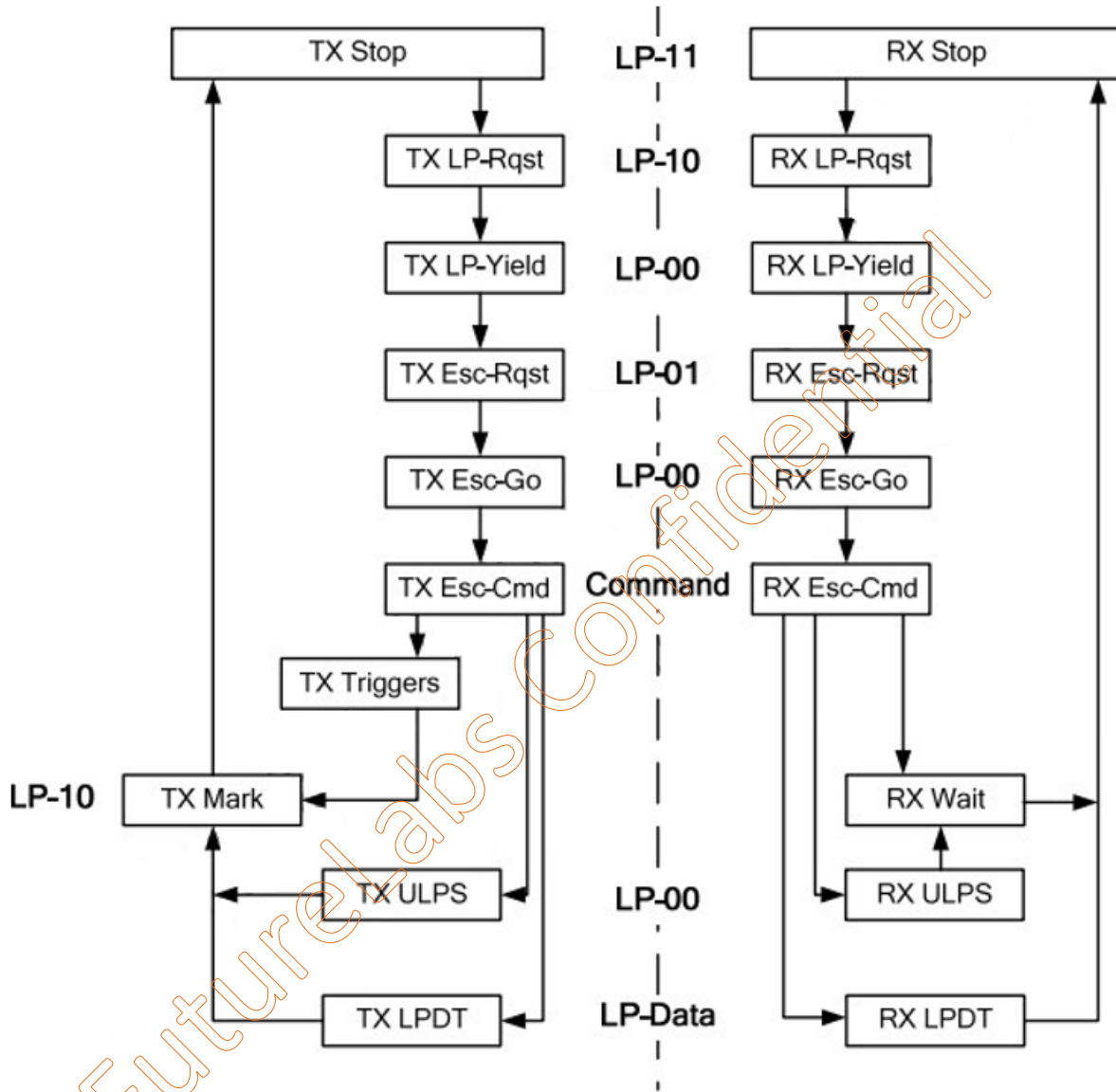
Once Escape mode is entered, the transmitter shall send an 8-bit entry code to indicate the requested action. The Entry Code as follows:

A. Tigger (Reset-Trigger(46h)), Tearing effect (Bah), Acknowledge (84h)
B. Drive Data Lane to Ultra Low Power State (78h)
C. Send Low Power Data Transmission (87h)
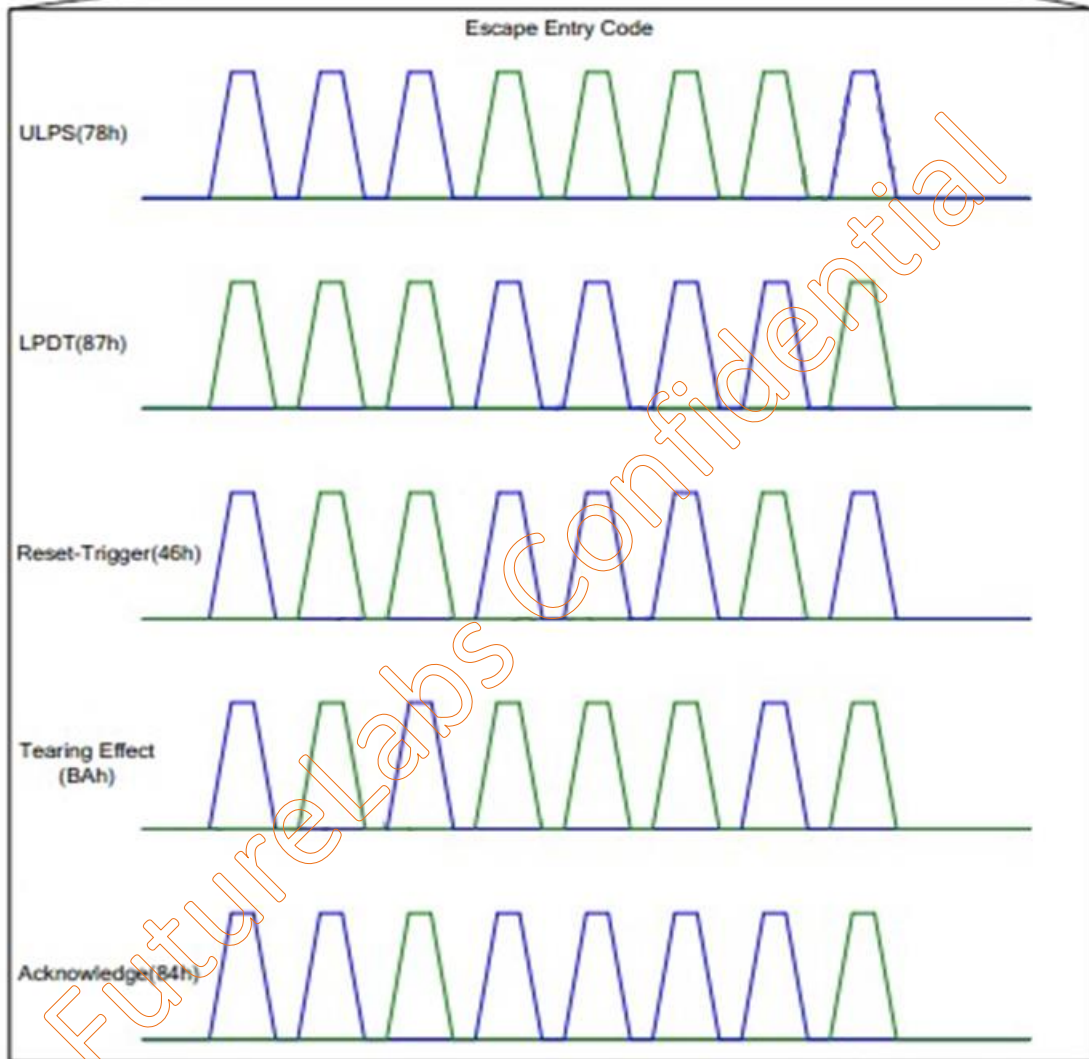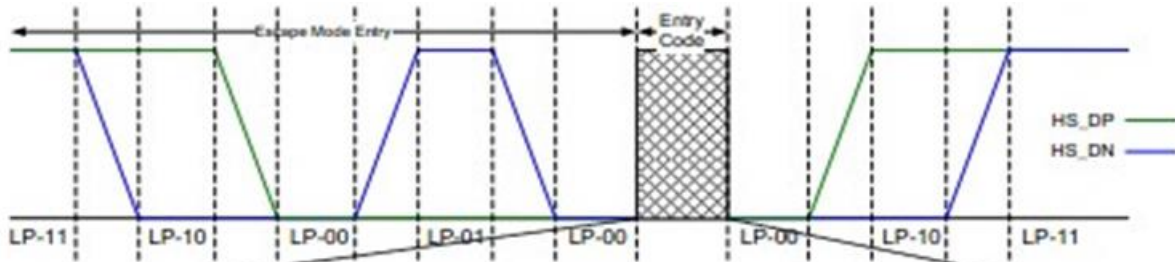
Escape mode timing sequence

3.3.5 High speed data transmission

The display module can enter high speed data transmission when Clock Lane in the High Speed Clock Mode. All Data Lane enter High Speed Data Transmission synchronously but may end at different time. Data Lane enters High Speed Data Transmission by the flow: LP-11→LP-01→LP-00→SoT (HS-00011101), and exits High Speed Data Transmission by the flow: Toggle the last payload data bit to different state immediately and keeps that state for a time $T_{HS-TRAIL}$.
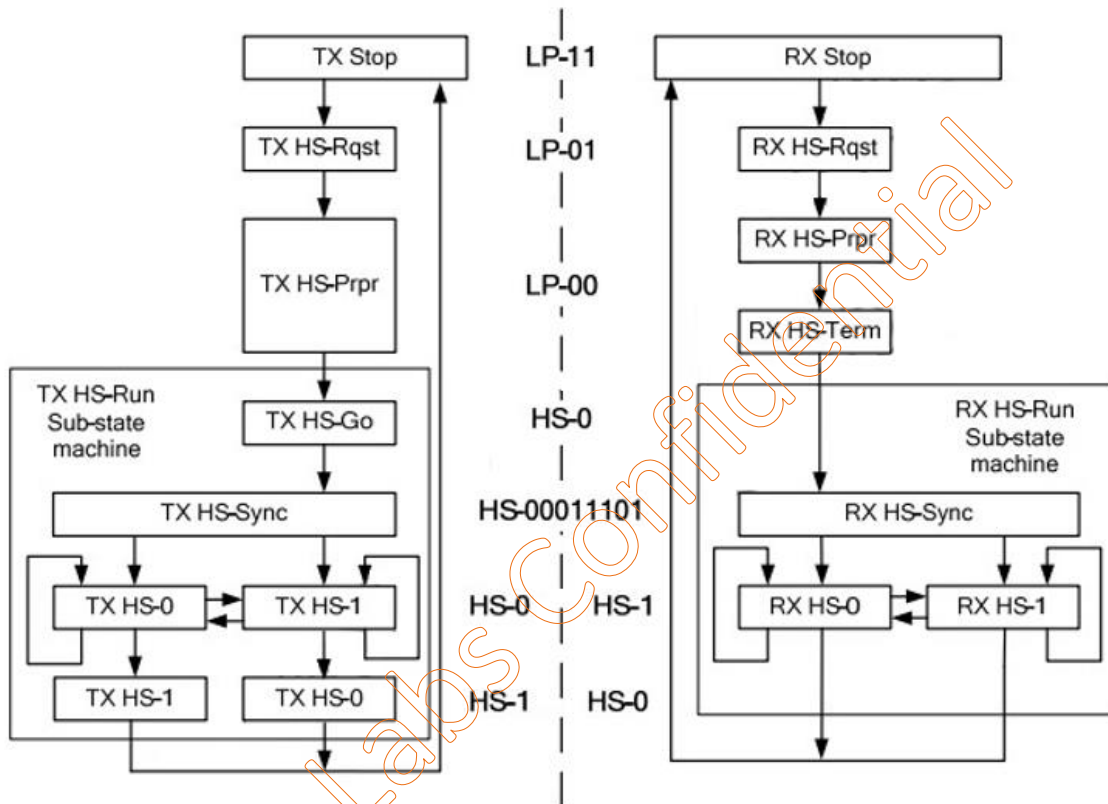
High speed data transmission state machine
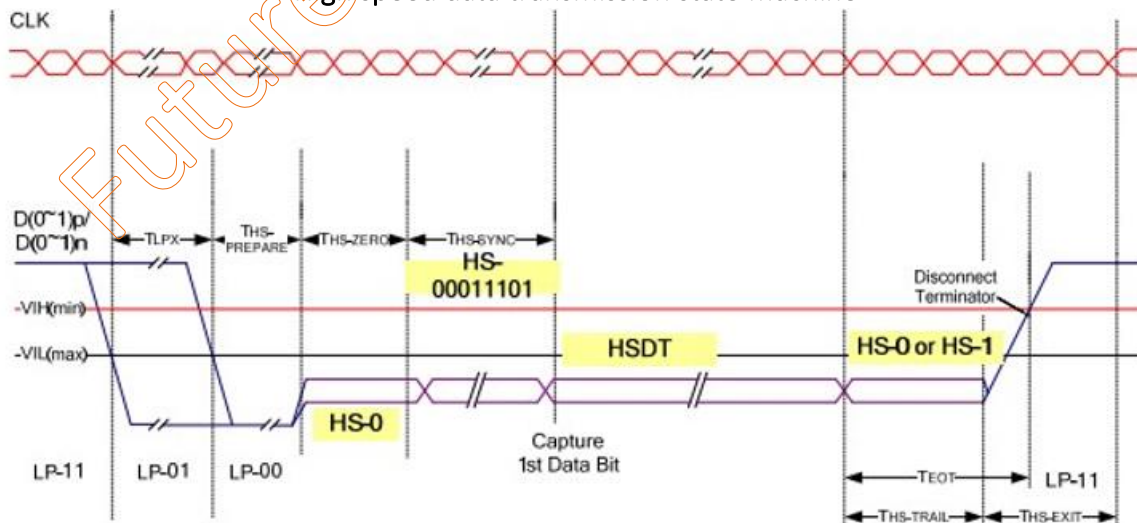
High Speed data transmission timing sequence
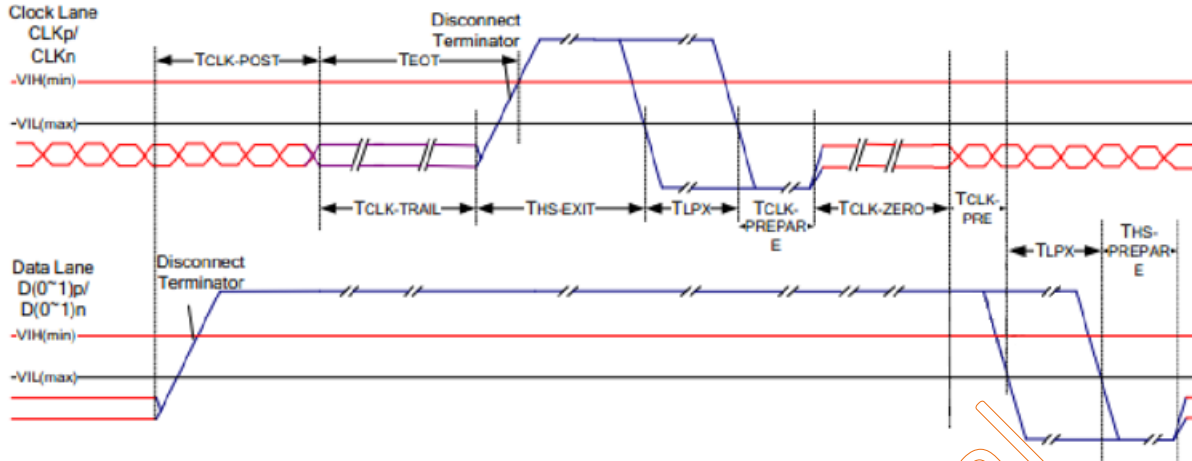
Switching the clock lane between clock transmission and LP mode

3.3.6 Bi-Directional data lane turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction.
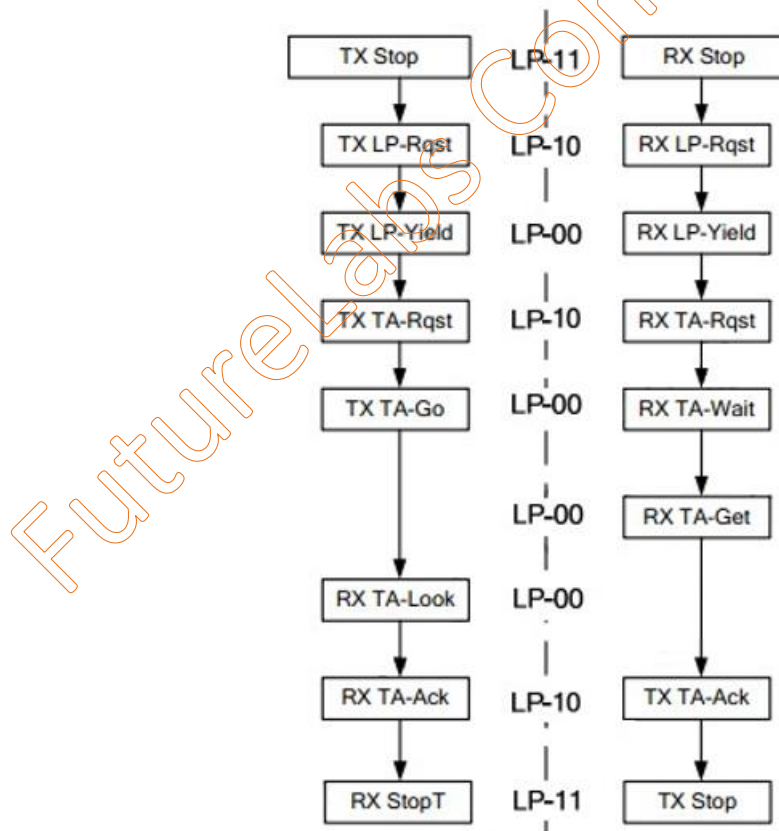
Turnaround State Machine
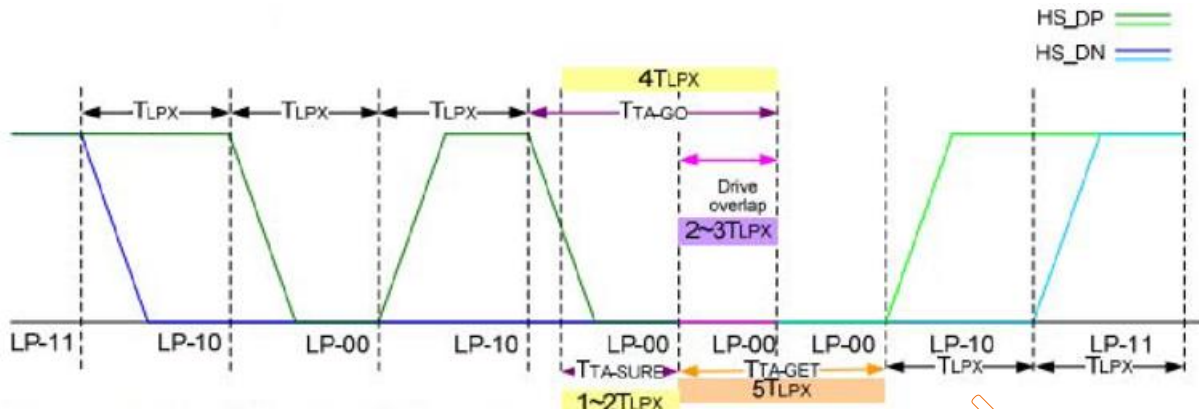
Note: (1) Ratio of TLPX(**Master**)/TLPX(**Slave**) is between 2/3~3/2

Turnaround Procedure

3.3.7 DSI Protocal

The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded with separate write commands at system startup.

LPS : Low power state
SOT : Start of Transmission
SP : Short Packet
LP : Long Packet
EOT : End of Transmission

Separate HS transmission packets

The packet includes two types which are Long packet and short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet.

Short packets shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length.
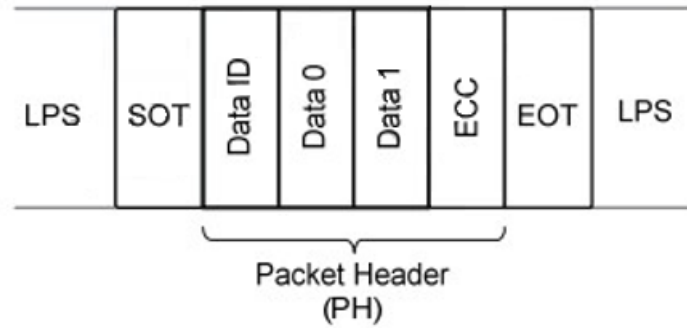
Packet Header
(PH)

DI (Data ID): Contain Virtual Channel Identifier and Data Type.

ECC (Error Correction Code): The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

Long packets specify the payload length using a two-byte Word Count Field and then the payload maybe from 0 to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data. The figure shows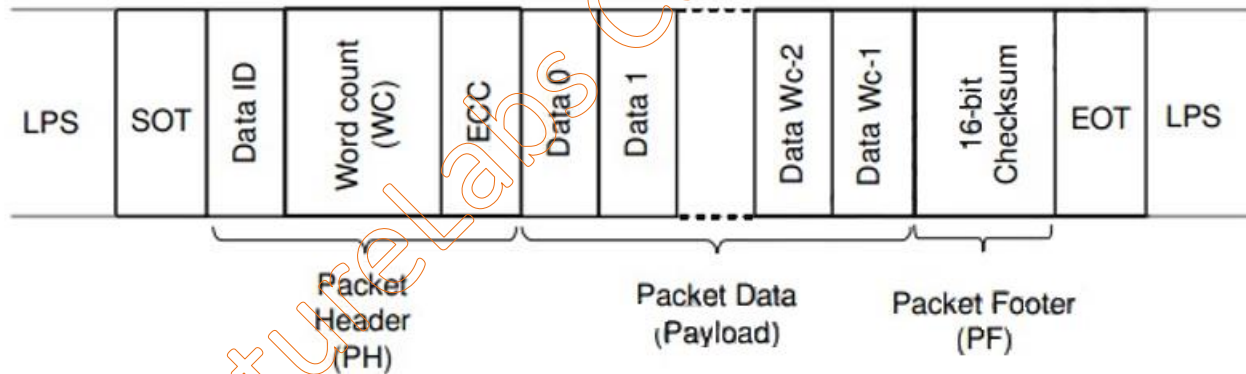 the structure of the long packet. Long packet header composed of three elements: an 8-bit Data Identifier, a 16-bit word count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

Where 65,541 bytes = (2^{16}-1)+4 bytes PH+2 bytes PF

DI (Data ID): Contain Virtual Channel Identifier and Data Type.

WC (Word Count): The Receiver use WC to define packet end.

ECC (Error Correction Code): The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

PF (Packet Footer): 16-bit Checksum.

According to packet form, basic elements include DI and ECC. Figure shows the format of Data ID.

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC (Virtual Channel)		DT (Data Type)					

DI[7:6]: These 2-bit identify the data as directed to one of four virtual channels.

DI[5:0]: These 6-bit specify the Data Type, which specifies the size, format and, in some cases, the interpretation of the packet contents.

Figure show short / Long packet command transmission sequence.

Short Packet writes Command / Parameters:
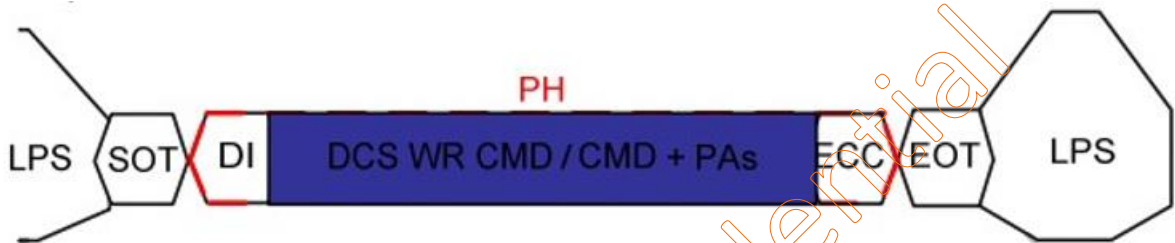
DI → Write suitable Data type.

EX: One CMD write, DI+DCS WR CMD

　　CMD + Pas write, DI+DCS WR CMD + Pas

Long Packet Write Command / Parameters / Pixel Data:

DI → Write suitable Data type.

WC → Write number of Payload Data.

Ex: One CMD write, WC setting as 1.

　　CMD + Pas write, WC setting as number of (CMD + Pas)

　　CMD + Data write, WC setting as number of (CMD + Pixel Data).

4.Timing Chart

4.1 Timing Table

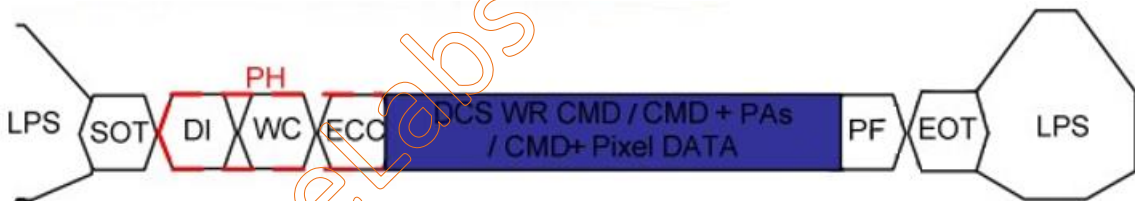| Item	Symbol	Min.	Typ.	Max.	Unit	Note
Clock Frequency	fclk	80.5	82.5	84.5	MHz	Frame rate=60Hz
Horizontal display area	thd		800		DCLK	
Horizontal Back Porch	HBP		100		DCLK	
Horizontal Pulse Width	HS		33		DCLK	
Horizontal Front Porch	HFP		100		DCLK	
HS Blanking	thb		233		DCLK	
HS period time	th		1033		DCLK	
Vertical display area	tvd		1280		H	
Vertical Back Porch	VBP		30		H	
Vertical Pulse Width	VS		2		H	
Vertical Front Porch	HFP		20		H	
VS Blanking	thb		52		H	
VS period time	tv		1332		H	

5. INTERFACE PIN DESCRIPTION

5.1 LCM Connector PIN Assignment

The electronics interface connector is **HIROSE** FH33J-40S-0.5H (10). (HIROSE), 40pin,pitch = 0.5mm

Pin No.	Symbol	I/O	Functions
1	NC	_	NC
2	VDDIN	P	Power input 3.3 Voltage
3	VDDIN	P	Power input 3.3 Voltage
4	GND	P	Power Ground
5	RST	I	Globel reset signal,low active
6	NC	-	No connection
7	GND	P	Power Ground
8	MIPI_0N	I	MIPI DSI differential data pair
9	MIPI_0P	I	MIPI DSI differential data pair
10	GND	P	Power Ground
11	MIPI_1N	I	MIPI DSI differential data pair
12	MIPI_1P	I	MIPI DSI differential data pair
13	GND	P	Power Ground
14	MIPI_CKN	I	MIPI DSI differential CLK pair
15	MIPI_CKP	I	MIPI DSI differential CLK pair
16	GND	P	Power Ground
17	MIPI_2N	I	MIPI DSI differential data pair
18	MIPI_2P	I	MIPI DSI differential data pair
19	GND	P	Power Ground
20	MIPI_3N	I	MIPI DSI differential data pair
21	MIPI_3P	I	MIPI DSI differential data pair
22	GND	P	Power Ground
23	NC	-	No connection
24	NC	-	No connection
25	GND	P	Power Ground
26	NC	-	No connection
27	PWMO	O	PWM control signal for BL driver

Pin No.	Symbol	I/O	Functions
28	NC	-	No connection
29	VCL	O	Output voltage pin
30	GND	P	Power Ground
31	LED-	P	Power for LED backlight negative
32	LED-	P	Power for LED backlight negative
33	NC	-	No connection
34	NC	-	No connection
35	NC	_	NC
36	NC	-	No connection
37	NC	-	No connection
38	NC	_	NC
39	VLED+	P	Power for LED backlight anode
40	VLED+	P	Power for LED backlight anode

Note: DGND=AGND=0V.

6. BLOCK DIAGRAM

The following diagram shows the functional block of the TFT module:
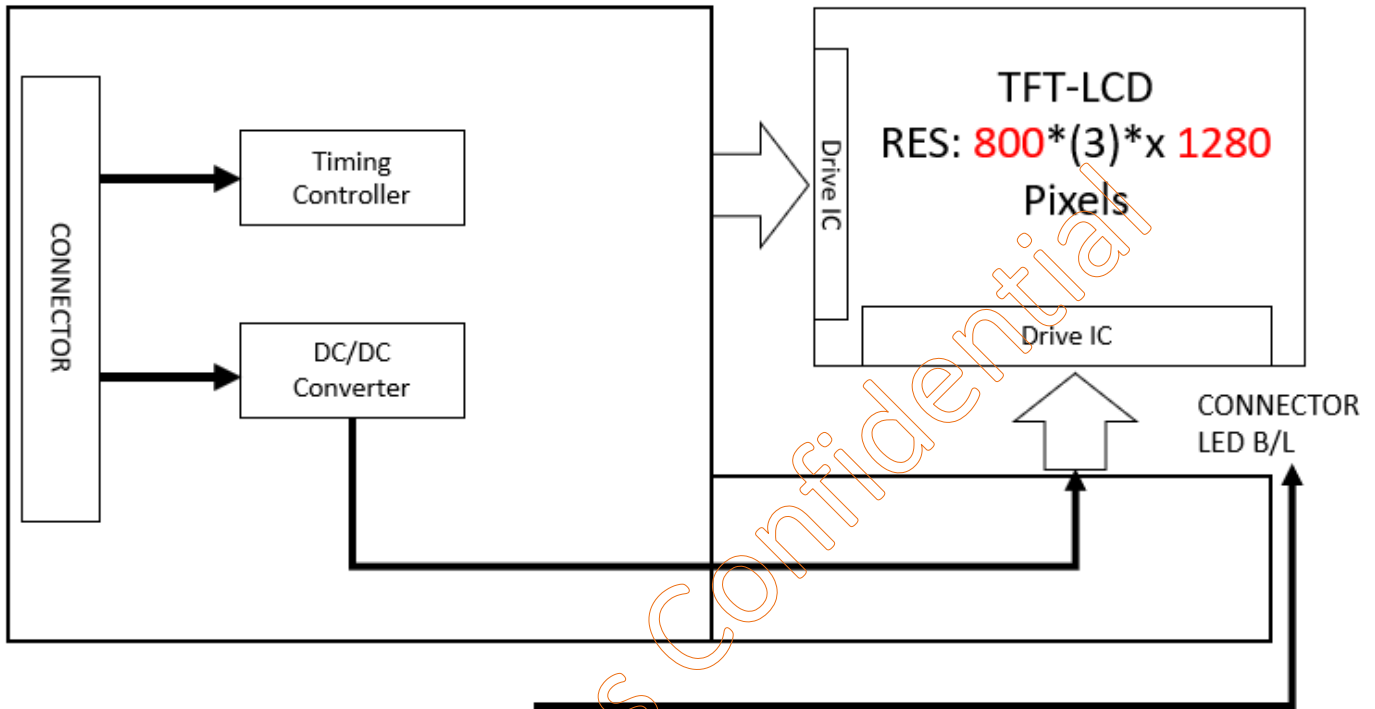
7. OPTICAL CHARACTERISTIC

The optical characteristics are measured under stable conditions at room temperature.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_X=0°$	600	800	-	-	(2)(5)
Response Time		T_R+T_F	25ºC	-	30	35	ms	(3)
Center Luminance of White		LC		400	450	-	cd/m2	(4)(5)
Uniformity		W			80		%	
Chromaticity	Red	Rx	$\theta_X=0°$, $\theta_Y=0°$ Viewing angle at normal direction	Typ. -0.04	TBD	Typ. +0.04	-	(1) (5)
		Ry			TBD		-	
	Green	Gx			TBD		-	
		Gy			TBD		-	
	Blue	Bx			TBD		-	
		By			TBD		-	
	White	Wx			0.31		-	
		Wy			0.32		-	
Viewing Angle	Horizontal	θ_{X+}	CR=10	85	85	-	Deg.	(1)(5)
		θ_{X-}		85	85	-		
	Vertical	θ_{Y+}		85	85	-		
		θ_{Y-}		85	85	-		

The following optical specifications shall be measured in a darkroom or equivalent state (ambient luminance <2 lux, and at room temperature), 15min. warm-up time

The room temperature is 25°C±2°C.

Note 1:   Definition of Viewing Angle

Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or the vertical clock direction with respect to the optical axis which is normal to the LCD surface
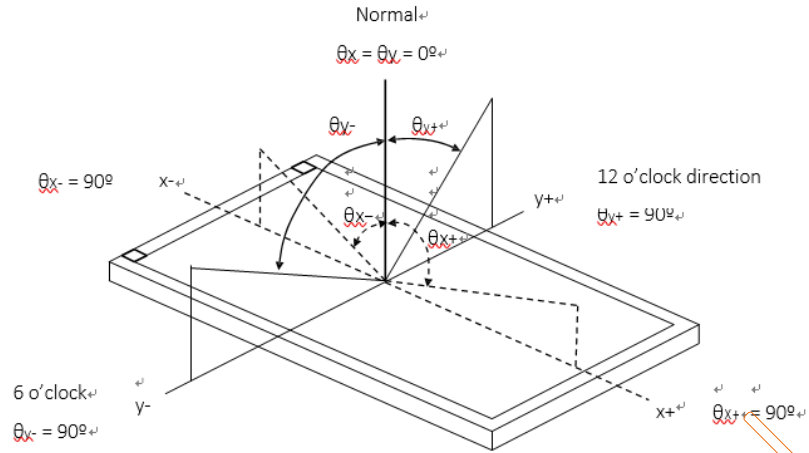
Note 2:   Definition of Contrast Ratio (CR)

Measure the viewing angle of Θ= 0 and at the center of the LCD surface. Luminance with all pixels in white state divide by Luminance with all pixels in Black state
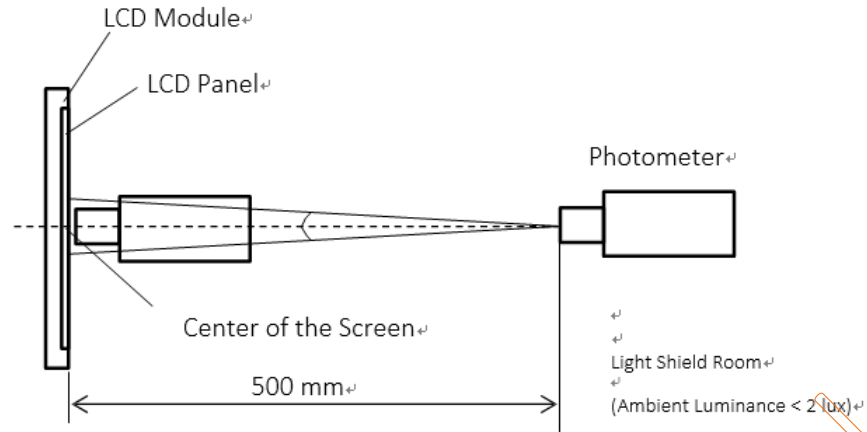
Note 3:   Definition of Response Time:

The response time is set initially by defining the "Rising Time (TR)" and the "Falling Time (TF)" respectively. Please refer the figure to the followings:
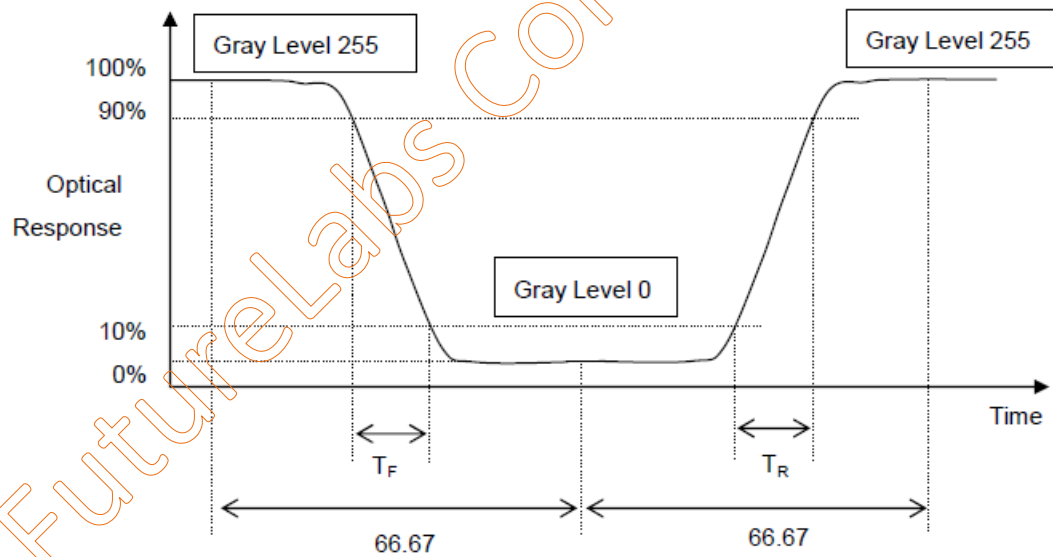
Note 4:   Definition of Brightness (L)

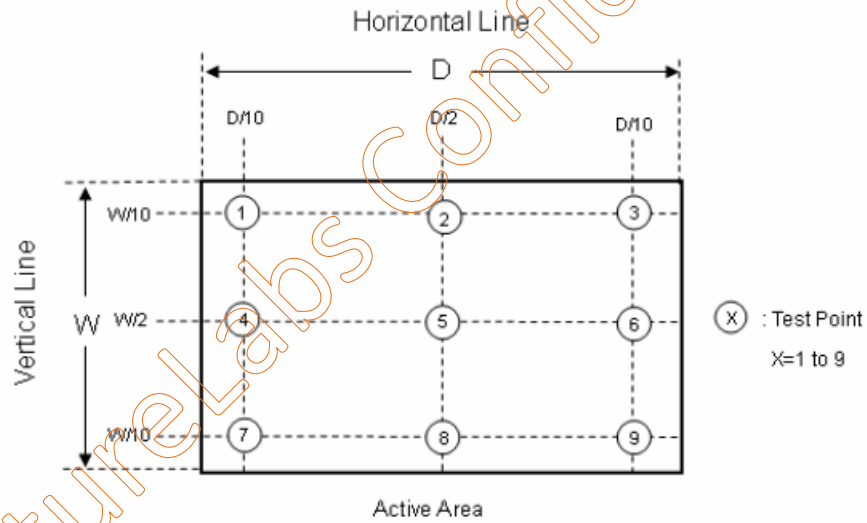Measure the center area of the panel and the viewing angle of the $\theta x=\theta y =0°$

Note 5:   The method of optical measurement:

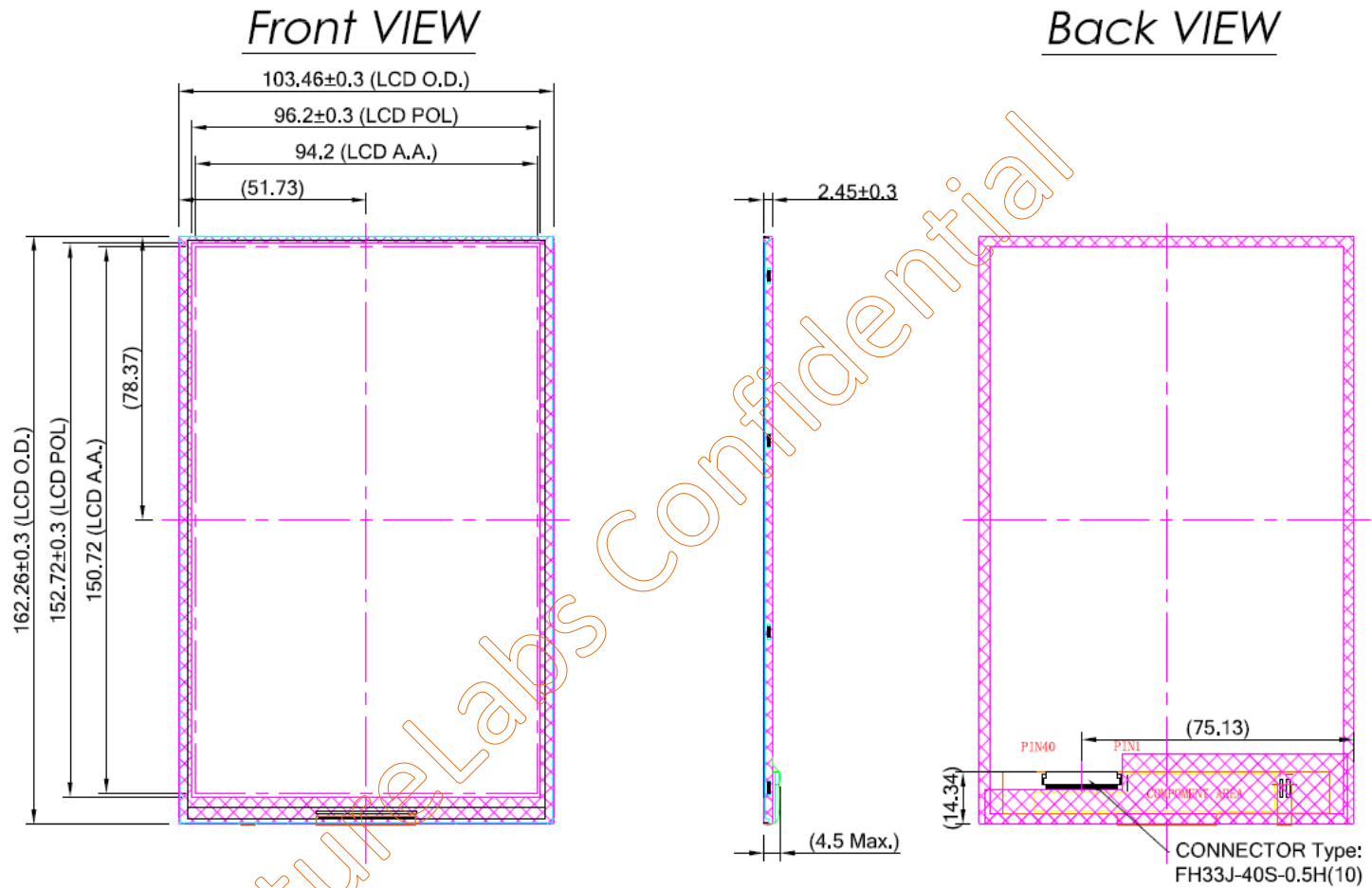Note 6:   Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points
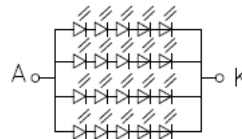
δW = Maximum [L (1), L (2), L (3), L (4)~ L (9)] / Minimum [L (1), L (2), L (3), L (4)~ L (9)]

8. DIMENSION AND DRAWING

Front VIEW

103.46±0.3 (LCD O.D.)
96.2±0.3 (LCD POL)
94.2 (LCD A.A.)
(51.73)

(78.37)

162.26±0.3 (LCD O.D.)
152.72±0.3 (LCD POL)
150.72 (LCD A.A.)

Back VIEW

2.45±0.3

(4.5 Max.)

(75.13)

PIN40   PIN1

(14.34)

CONNECTOR Type:
FH33J-40S-0.5H(10)

LED CIRCUIT DIAGRAM:

A o————o K

Pin Define

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	NC	11	MIPI-1N	21	MIPI-3P	31	VLED-
2	VDD	12	MIPI-1P	22	GND	32	VLED-
3	VDD	13	GND	23	NC	33	NC
4	GND	14	MIPI-CKN	24	NC	34	NC
5	Reset	15	MIPI-CKP	25	GND	35	NC
6	NC	16	GND	26	NC	36	NC
7	GND	17	MIPI-2N	27	PWMO	37	NC
8	MIPI-0N	18	MIPI-2P	28	NC	38	NC
9	MIPI-0P	19	GND	29	VCL	39	VLED+
10	GND	20	MIPI-3N	30	GND	40	VLED+

9. PRECAUTION AND PRODUCT HANDLING

- Do not apply the external force such as bending or twisting to the LCD panel and backlight during assembly.
- Do not insert and plug out the input connector while the LCD panel is operating.
- Do not take apart the panel or frame from LCD module assembly or insert anything into the backlight unit.
- Do not keep the same pattern in a long period of time, it may cause image sticking on LCD panel. Can use shuffle content periodically if fixed pattern is displayed on the screen.
- Do not touch the display area with bare hands, this will stain the display area.
- Pay attention to handle lead wire of backlight, that is not tugged in connect with LED driver.
- Do not change variable resistance settings in LCD panel, it may cause not satisfy of LCD characteristics specification.
- The surface of LCD panel's polarizer is very soft and easily scratched, please use a very soft dry cloth without chemicals for cleaning.
- To avoid the static electricity to damage the CMOS LSI, the operator should be grounded when in contact with the LCD panel, and also to all electrical equipment.
- Need to follow the correct power frequency when LCD panel is connecting and operating, this can avoid damage to CMOS LSI during latch-up.
- Need to store the LCD panel indoor without the exposure of sunlight where the temperature is 25°C ± 5°C and the humidity is below 60% RH.