Approval Sheet

■ **Preliminary specification**

□ **Final specification**

Customer Name	* * * * * *
Product Description	**3.5inch 1440RGB*1600 TFT-LCD Module**
Version	**Pre.0**
Supplier	**BOE**
Module Code	VS035ZSM-NW0-69P0

Customer Approval		**BOE Approval**	
SIGNATURE/TITLE	**DATE**	**SIGNATURE/TITLE**	**DATE**
PREPARED BY		**PREPARED BY**	
_____/_____	_____	_____/_____	_____
REVIEWED BY		**REVIEWED BY**	
_____/_____	_____	_____/_____	_____
APPROVED BY (R&D)		**APPROVED BY (R&D)**	
_____/_____	_____	_____/_____	_____
APPROVED BY (QA)		**APPROVED BY (QA)**	
_____ _/_____	_____	_____ _/_____	_____

ORDOS YUANSHENG
OPTOELECTRONICS TECHNOLOGY CO.,LTD.

Product Specification

Product Name : 3.5" TFT-LCD Module

Model Name : VS035ZSM-NW0-69P0

Description : 3.5" 1440RGB×1600 16.7M Color

PREPARED BY	CHECKED BY	APPROVALED BY

ORDOS YUANSHENG
OPTOELECTRONICS TECHNOLOGY CO.,LTD.

Revision History

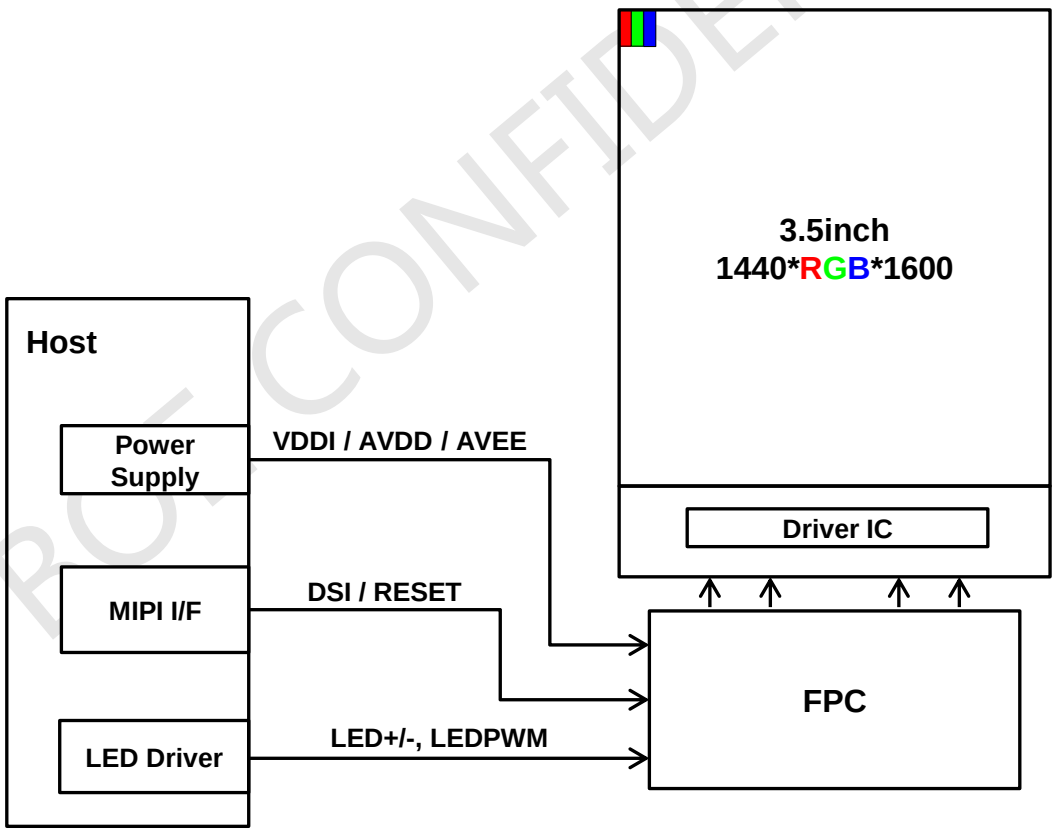
REV.	ECN NO.	DESCRIPTION OF CHANGES	DATE	PREPARED
P0	-	Initial Release	2017.03.20	GONG LEI

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

The 3.5inch TFT-LCD Module is a Color Active Matrix TFT LCD panel using LTPS (Low Temperature Poly-silicon) TFT's (Thin Film Transistors) as an active switching devices. This module has a 3.5 inch diagonally measured active area with 1440*1600 resolutions (1440 horizontal by 1600 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.



1.2 Features

- High PPI
- Fast response time
- High frame ratio
- High luminance, low reflection and wide viewing angle
- RoHS、Halogen Free Compliant

1.3 Application

- Virtual Reality Device
- Augmented Reality Device

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remark
Display method	Active matrix TFT		
Display mode	Transmission mode, Normally black		
Screen size	3.5 (88.79mm)	inch	diagonally
Number of pixels	1440(H) × 1600(V)	pixels	615 ppi
Active area	59.4(H) × 66.0(V)	mm	
Pixel pitch	13.75(H) × 41.25(V)	um	
Pixel arrangement	RGB stripe		
Display colors	16.7M	colors	8bit
NTSC Ratio	85%		
LCM Outline Dimension	62.2(H) × 73.6(V) × 1.7 (T)	mm	Note 1)
LCM Weight	17.0 ±2.0	gram	
Driver IC	NT57860		
Interface	MIPI DSI (Video Mode)		
Surface Treatment	HC, ≥3H		

Note:

1) Protection film is not included.

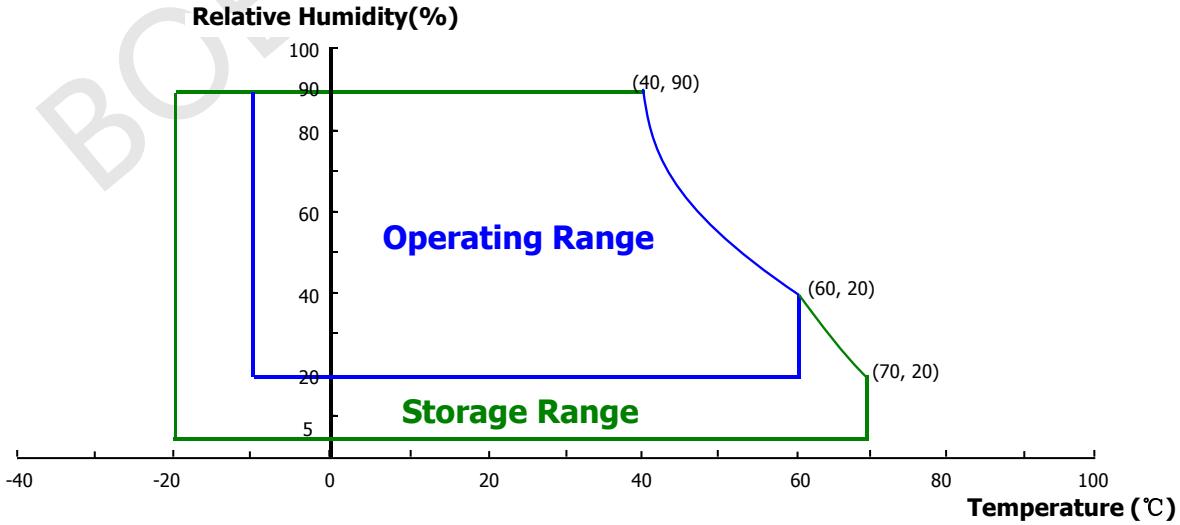
2.0 ABSOLUTE MAXIMUM RATINGS

< Table 2. Absolute Maximum Ratings> [Ta =25±2 ℃]

Items	Symbol	Rating	Unit	Remark
Logic voltage	VDDI	-0.3 to +1.8	V	
Positive Analog Power Supply Voltage	AVDD	-0.3 to +5.7	V	
Negative Analog Power Supply Voltage	AVEE	-5.7 to +0.3	V	
LED forward current	I_{LED}	50	mA	each LED 10% on duty
Storage temperature	T_{STG}	-40 to +70	℃	
Operation temperature	T_{OPR}	-10 to +55	℃	
Humidity (ambient temeprature=Ta)	Ta≤55℃, 90% RH Max.			

Note 1: If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop. It is not allowed for any of these ratings to be exceeded. Make sure all the design characte ristics are adequate before the panel is initialed.

Note 2: Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 55 ℃ max. and no condensation of water.



3.0 ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Panel

< Table 3. LCD Panel Electrical Specifications > [Ta =25±2 ℃]

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Logic voltage		VDDI	1.7	1.8	1.9	V	Note 1
Positive Analog Power Supply Voltage		AVDD	5.4	5.7	6.0	V	
Negative Analog Power Supply Voltage		AVEE	-6.0	-5.7	-5.4	V	
Frame Ratio		FPS	-	90		Hz	
Input signal voltage	High level	V_{IH}	0.7×VDDI	-	VDDI	V	
	Low level	V_{IL}	VSSI	-	0.3×VDDI	V	
Output signal voltage	High level	V_{OH}	0.8×VDDI	-	VDDI		
	Low level	V_{OL}	VSSI	-	0.2×VDDI		
Current consumption		I_{VDDI}	-	70	-	mA	Note 2
		I_{AVDD}	-	10.5	-	mA	
		I_{AVEE}	-	-9.5	-	mA	
Driver IC ESD		HBM	- 2	-	+2	kV	
		MM	-200	-	+200	V	

Note 1:
The value can be adjusted by software to optimize display quality.
The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during operation. To prevent noise, a bypass capacitor must be inserted into the line close to power pin. Please make sure all the design settings are used within this range before the panel is initialed.

Note 2:
Test pattern: All White Display

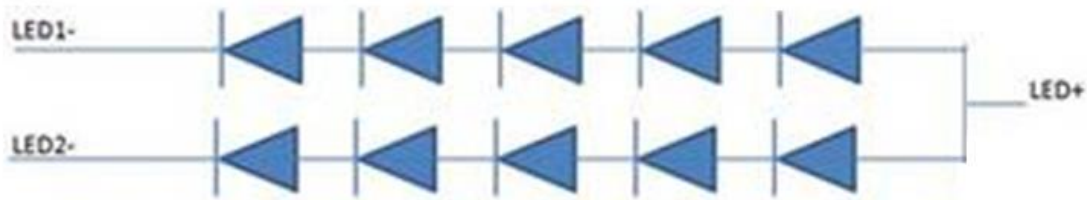
3.2 Back-light Unit

< Table 4. LED Driving Specifications > Ta=25+/-2°C

Items	Symbol	Min.	Typ.	Max.	Unit	Remark
Forward Current	If	-	50	-	mA	Note1
Forward Voltage	Vf	-	6.5	-	V	Note1
Power Consumption	P_{BL}	-	325	-	mW	Note2
LED Q'ty			10		Ea	

Note 1: The driving condition is defined for each LED chip.
Note 2: The B/L power consumption is defined for the backlight module.
the schematic drawing of the backlight unit is as the figure.
The B/L power consumption is based on 10% on duty mode

Ref. Total power consumption(max) depends on LED current/LED driver efficiency, etc.



Back-Light Circuit

4.0 OPTICAL SPECIFICATION

4.1 Overview

The optical characteristics should be measured in a dark room (ambient luminance≤ 1 lux and temperature = 25±2℃) with the equipment of Konica Minolta CA-310 and CS-2000 and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0° . The center of the measuring spot on the display surface should stay fixed.
The operation should be under the recommended operating conditions.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle	Horizontal	θ_3	CR > 10	-	70	-	degree	Note 1
		θ_9		-	70	-		
	Vertical	θ_{12}		-	70	-		
		θ_6		-	70	-		
Color Gamut (NTSC)			θ = 0°	-	85	-	%	
Contrast Ratio		CR	θ = 0°	-	600	-		Note 2
Luminance of White	Center	Y_w	θ = 0°	120	150	-	cd/m^2	Note 3
Luminance Uniformity	5 Points	ΔY5		80%	85%	-		Note 4
Chromaticity (CIE 1931)	Red	Rx	θ = 0°	-	0.66	-		Note 5
		Ry		-	0.372	-		
	Green	Gx		-	0.275	-		
		Gy		-	0.652	-		
	Blue	Bx		-	0.15	-		
		By		-	0.06	-		
	White	Wx		-	0.299	-		
		Wy		-	0.315	-		
Response Time (G to G)		T	θ = 0°	-	-	5	ms	Note 6
Flicker			θ = 0°	-	-	-30	db	Note 7
Cross Talk		CT	θ = 0°	-	-	2	%	Note 8

Note 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (FIGURE 1).

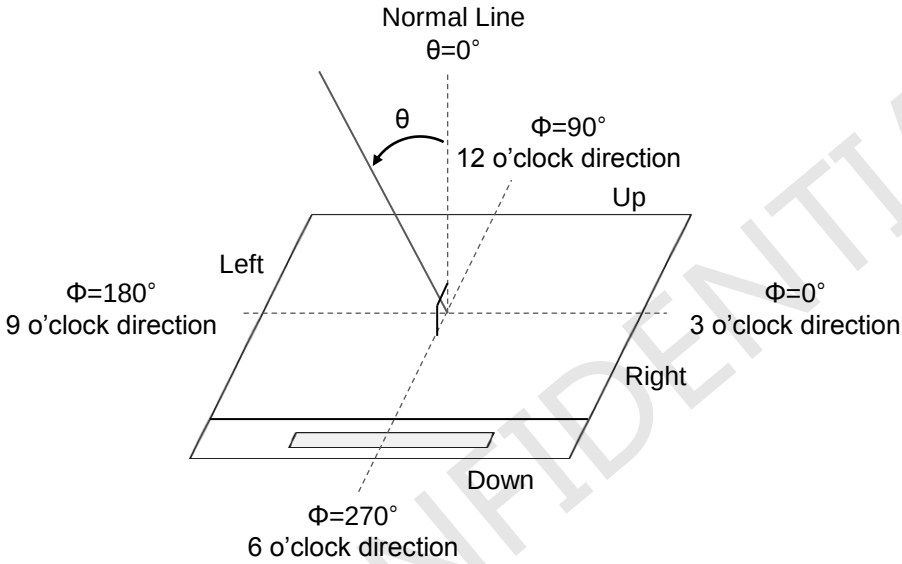


Fig.1 Viewing angle measurement setup

Note 2. Contrast ratio measurements shall be made at viewing angle of θ=0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state (FIGURE 1).
Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 3. Luminance of white is defined as luminance values of the center point across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display. The luminance is measured by CA310 when **the LED current is set at 50mA/ea and the backlight is under the 10% on duty mode.**

Note 4. The White luminance uniformity is then expressed as:
ΔY = Minimum Luminance of 5 points / Maximum Luminance of 5 points (FIGURE 3).

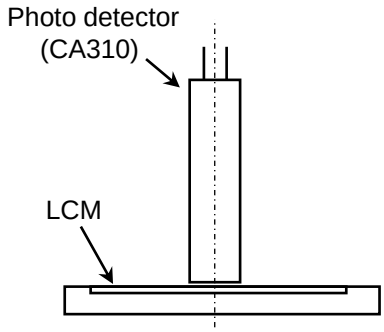


Fig.2 Luminance, uniformity & chromaticity measurement setup

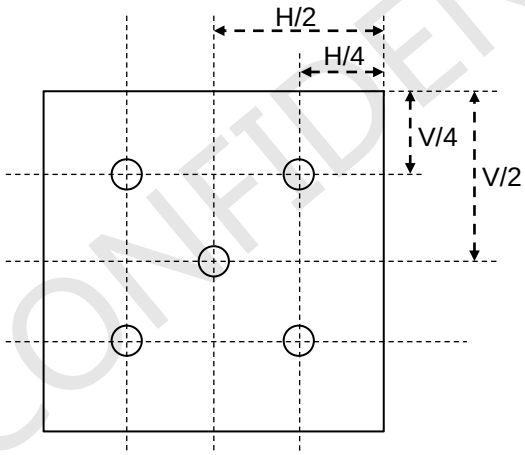


Fig.3 Luminance uniformity measurement setup

Note 5. The color chromaticity is measured with all pixels first in red, green, blue and white. Measurements should be made at the center of the panel.

Note 6. Definition of Response time.

The output signals of photo detector are measured when the input signals are switched between different display pattern (Gray-to-Gray).

The response time is defined as the time interval **between the 10% and 90% of amplitudes** (Fig.4)

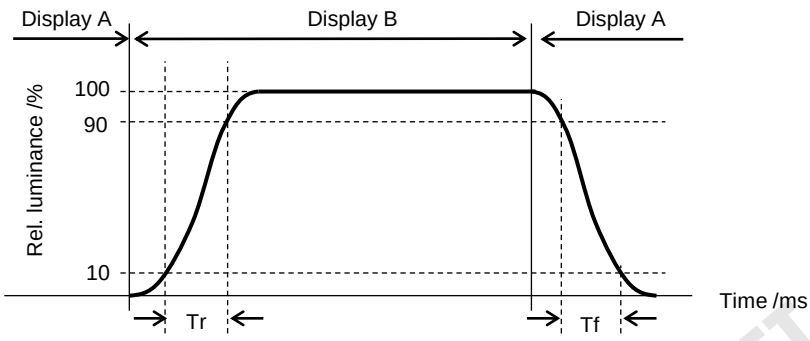


Fig.4 Response Time

Note 7. Flicker

Test equipment: CA310
Test pattern: column inversion (Fig.5)

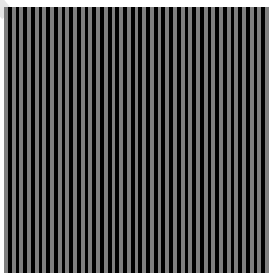


Fig.5 Flicker pattern

Note 8. Cross Talk

Test pattern: Fig.6

$$Xtalk = \max\left(\frac{|Y1-Y2|}{Y1}, \frac{|Y3-Y4|}{Y3}\right)$$

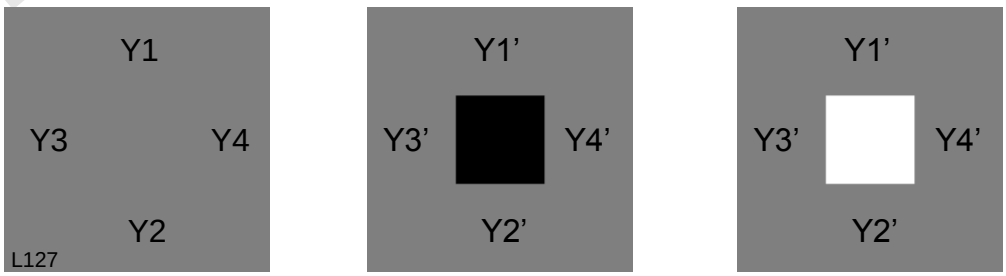


Fig.6 Cross-talk pattern

5.0 INTERFACE CONNECTION

The electronics interface connector is **Kyocera 145863050024829+**
The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

NO.	Symbol	Description	NO.	Symbol	Description
1	GND1	Ground	26	DSI_D2P_A	MIPI DSI port A data 2_P
2	IOVDD	1.8V	27	GND	Ground
3	VSP	5.7V	28	GND	Ground
4	IOVDD	1.8V	29	DSI_CLKP_B	MIPI DSI port B clock_P
5	GND	Ground	30	DSI_D1P_B	MIPI DSI port B data 1_P
6	ID0	GND	31	DSI_CLKN_B	MIPI DSI port B clock_N
7	VSN	-5.7V	32	DSI_D1N_B	MIPI DSI port B data 1_N
8	ID1	IOVDD	33	GND	Ground
9	GND	Ground	34	GND	Ground
10	GND	Ground	35	DSI_D3P_B	MIPI DSI port B data 3_P
11	DSI_D0N_A	MIPI DSI port A data 0_N	36	DSI_D0P_B	MIPI DSI port B data 0_P
12	DSI_D3N_A	MIPI DSI port A data 3_N	37	DSI_D3N_B	MIPI DSI port B data 3_N
13	DSI_D0P_A	MIPI DSI port A data 0_P	38	DSI_D0N_B	MIPI DSI port B data 0_N
14	DSI_D3P_A	MIPI DSI port A data 3_P	39	GND	Ground
15	GND	Ground	40	GND	Ground
16	GND	Ground	41	LED +	LED anode
17	DSI_D1N_A	MIPI DSI port A data 1_N	42	RESET	LCD reset signal (low active)
18	DSI_CLKN_A	MIPI DSI port A clock_N	43	GND	Ground
19	DSI_D1P_A	MIPI DSI port A data 1_P	44	TE	Tearing effect output pin
20	DSI_CLKP_A	MIPI DSI port A clock_P	45	LED 1-	LED cathode 1
21	GND	Ground	46	GND	Ground
22	GND	Ground	47	LED 2-	LED cathode 2
23	DSI_D2P_B	MIPI DSI port B data 2_P	48	LEDPWM	LED PWM signal pin
24	DSI_D2N_A	MIPI DSI port A data 2_N	49	GND	Ground
25	DSI_D2N_B	MIPI DSI port B data 2_N	50	GND	Ground

Remark:
Port A&B are determined by the value of BA register :
When BA Register is assigned to 07 ,only port A is valid
When BA Register is assigned to 03, port A and B are valid.

VDDI is defined as “H” level and GND is defined as “L” level.

6.0 Block Diagram

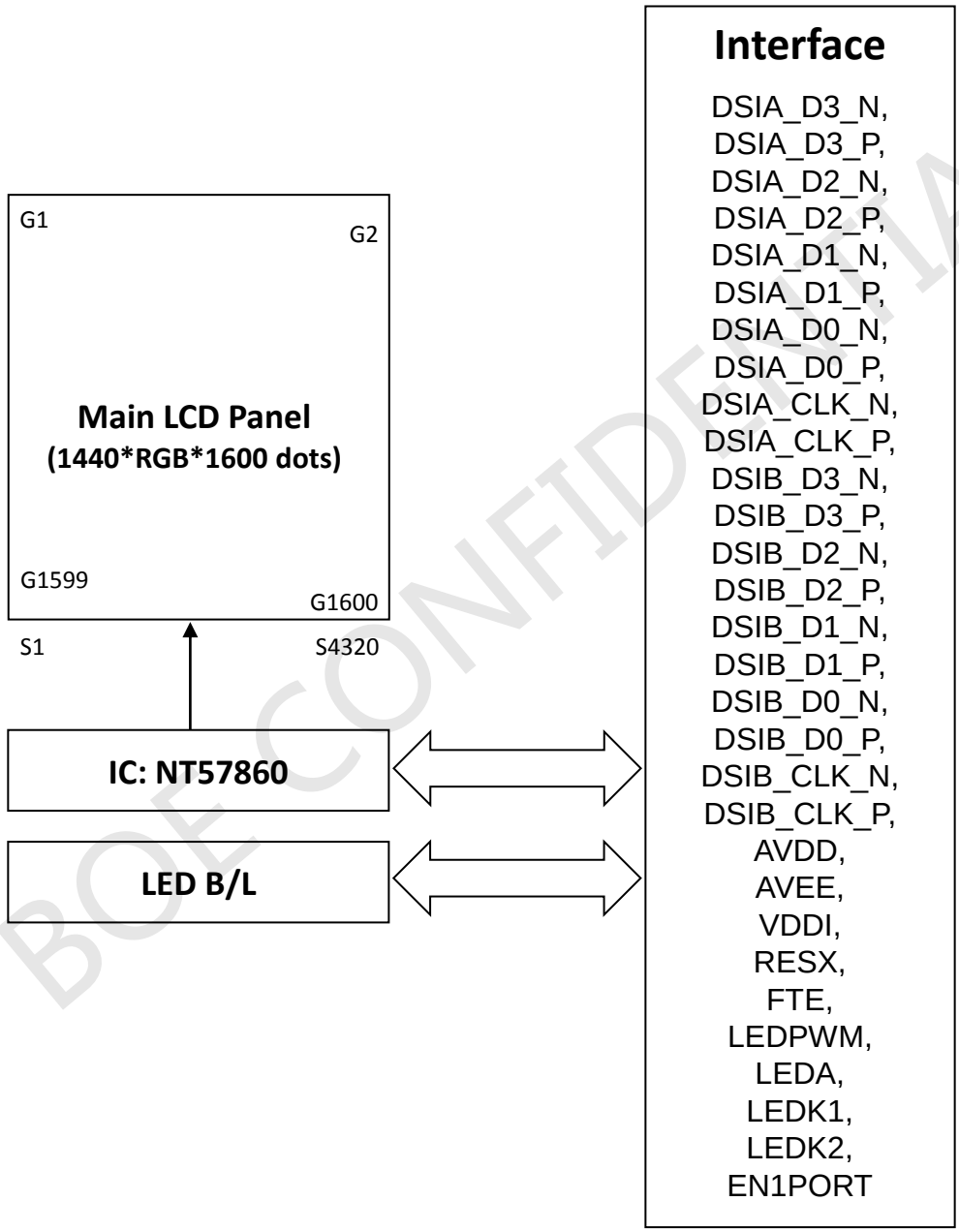
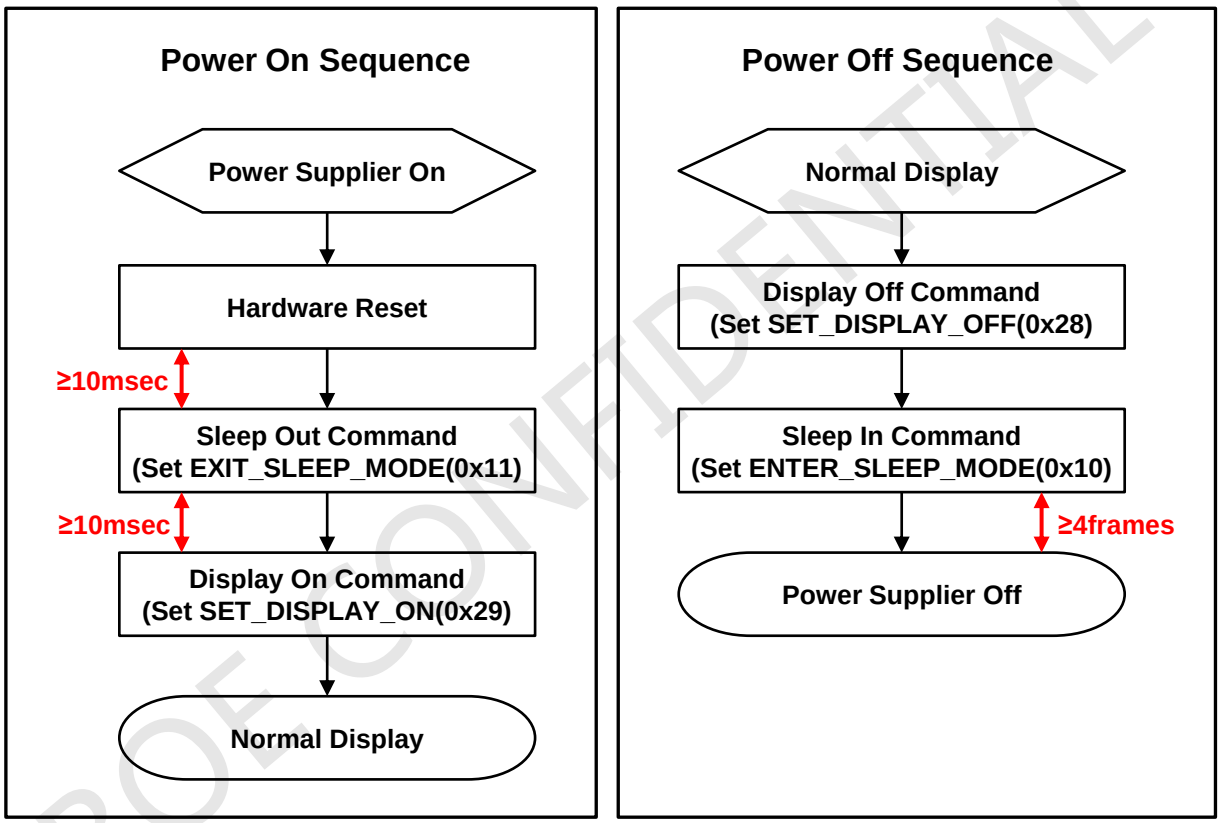


Figure 5. Block diagram

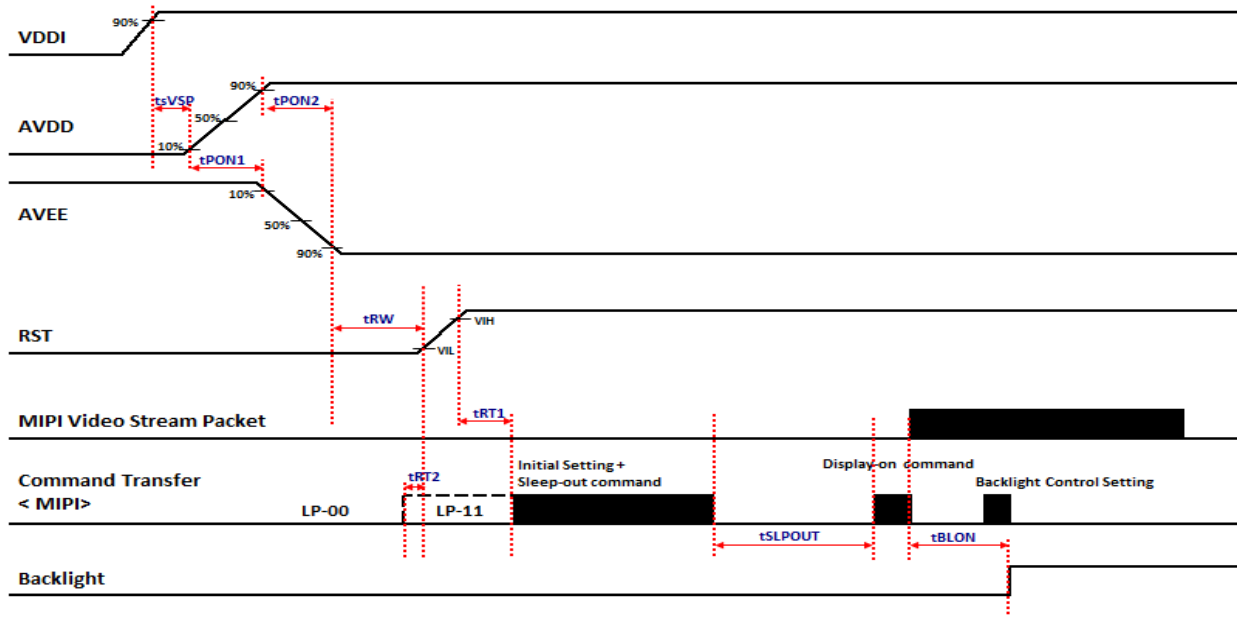
7.0 Timing Characteristics

7.1 Power On/Off Sequence

The power supply ON/OFF setting for Display ON/OFF, Standby Set/Exit, and Sleep Set/Exit sequences is illustrated in figure below.



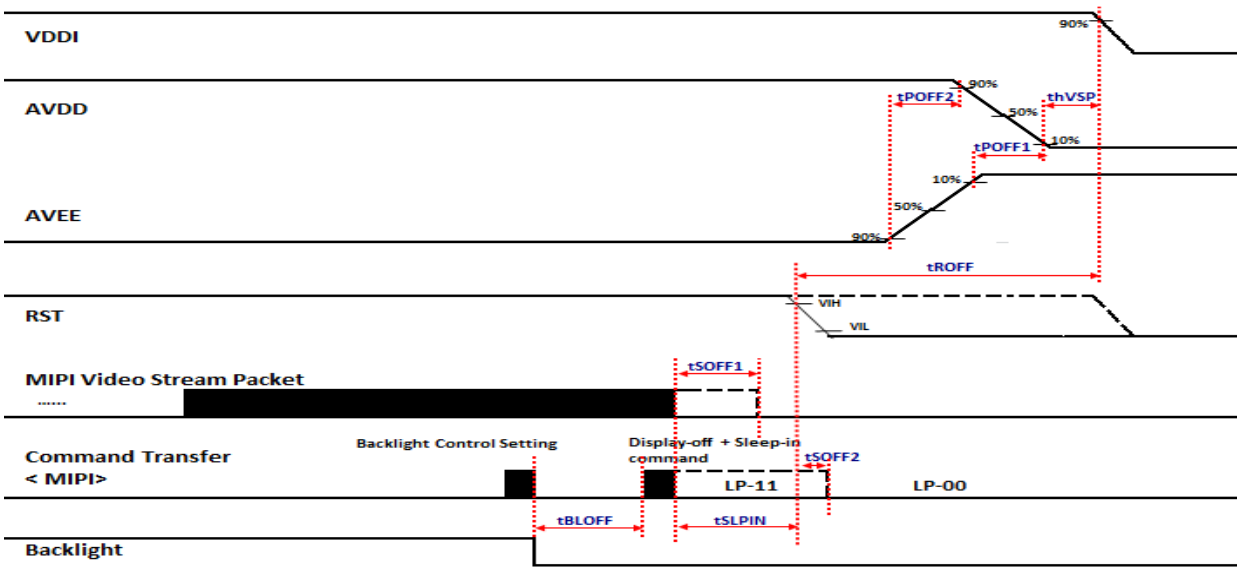
■ **Power On Sequence**



Note 1: After Sleep-Out Command, Driver IC will reload MTP registers and do internal power on action. Therefore, any initial settings (such as 3Ah,3Bh,etc.) by MIPI should be set after Sleep-Out command with minimum delay time 100ms.

Note 2: When RST keep low, MIPI lanes must go to LP00 state to avoid leakage current!! When RST goes to high, MIPI lanes must go to LP11 state.

■ **Power Off Sequence**



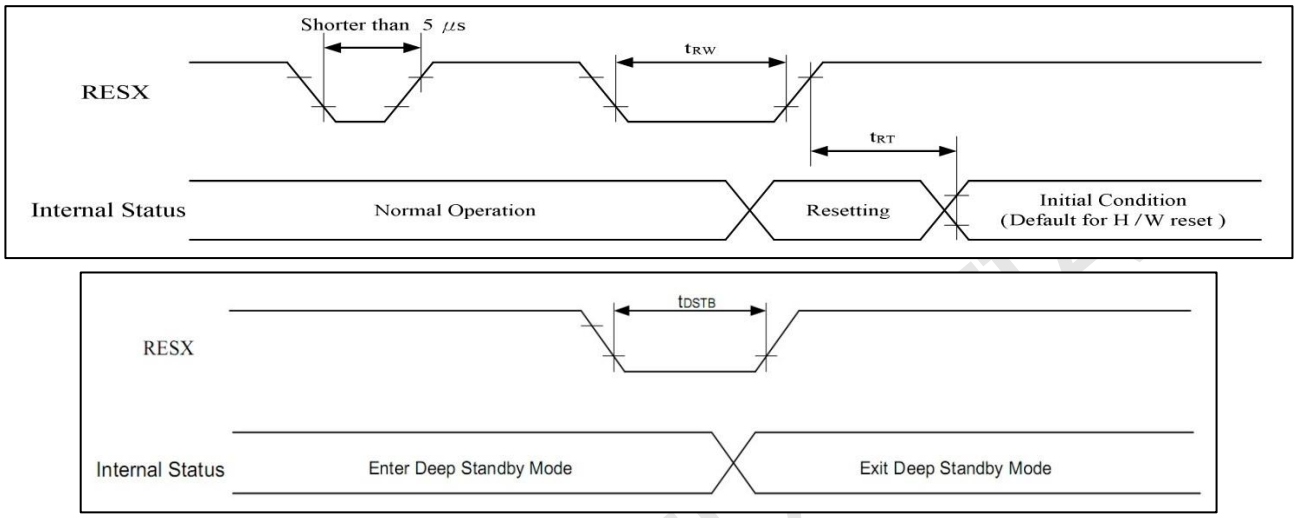
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
AVDD - AVEE delay time (10% to 10%)	tPON1	Power On	0	-	-	us
AVDD - AVEE delay time (90% to 90%)	tPON2	Power On	0	-	-	us
VDDI On to AVDD On time (90% to 10%)	tsVSP	Power On	1	-	-	ms
All Power On to RST Hi-level time (90% to VIL)	tRW	Power On	10	-	-	ms
RST Hi-level (VIH) to 1st Command time	tRT1	Power On	10	-	-	ms
(MIPI goes to LP11 state) to RST goes to High-level (VIL)	tRT2	Power On	0	-	-	us
SLPOUT Sequence Request time	tSLPOUT	Power On	100	-	-	ms
Display On Command to BL On time	tBLON	Power On	40	-	-	ms
AVDD - AVEE delay time (10% to 10%)	tPOFF1	Power Off	0	-	-	us
AVDD - AVEE delay time (90% to 90%)	tPOFF2	Power Off	0	-	-	us
AVDD Off to VDDI Off time (10% to 90%)	thVSP	Power Off	0	-	-	us
RST Low to VDDI Off time (VIH to 90%)	tROFF	Power Off	0	-	-	us
BL Off to Display Off Command time	tBLOFF	Power Off	0	-	-	us
SLPIN Sequence Request time	tSLPIN	Power Off	60	-	-	ms
SLPIN Finished to MIPI Video Stream Off	tSOFF1	Power Off	0	-	-	us
RST goes to Low-level (VIH) to (MIPI goes to LP00 state)	tSOFF2	Power Off	0	-	-	us

About the "H" level and "L" level definition, please refer to the below table:

Input / Output					
Item	Symbol	Min.	Typ.	Max.	Unit
Logic High level input voltage *(Except RESX)*	VIH	0.7VDDI	-	VDDI	V
Logic Low level input voltage *(Except RESX)*	VIL	VSS	-	0.3VDDI	V
Logic High level input voltage *(RESX)*	VIH	0.8VDDI	-	VDDI	V
Logic Low level input voltage *(RESX)*	VIL	VSS	-	0.2VDDI	V
Logic High level input voltage *(ENPWRP/N)*	VIH	0.7AVDD	-	AVDD	V
Logic Low level input voltage *(ENPWRP/N)*	VIL	AVSS	-	0.3AVDD	V

Note 1: VDDI=1.7 to 1.9V, AVDD=5.4 to 6.0V, AVEE=-6.0 to -5.4V, AVSS=VSS=0V, Ta=-40℃ to 70℃ (to +85℃ no damage)

7.2 Reset Input Timing



(VSS=VSSI=DVSS=0V, VDDI=1.65V to 1.95V, VDDAM=1.65V to 1.95V)

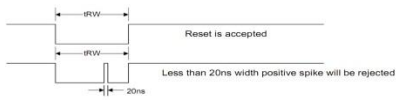
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit
RESX	t_{RW}	Reset pulse duration (Note 1)	10	-	-	ms
	t_{RT}	Reset cancel (Note 2)	-	-	10	ms
			-	-	120	ms
	t_{DSTB}	Reset pulse duration	10	-	-	ms

Note：

- *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers.*
  This loading is done every time when there is HW reset cancel time (tRT) within 10 ms after a rising edge of RESX.
- *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:*

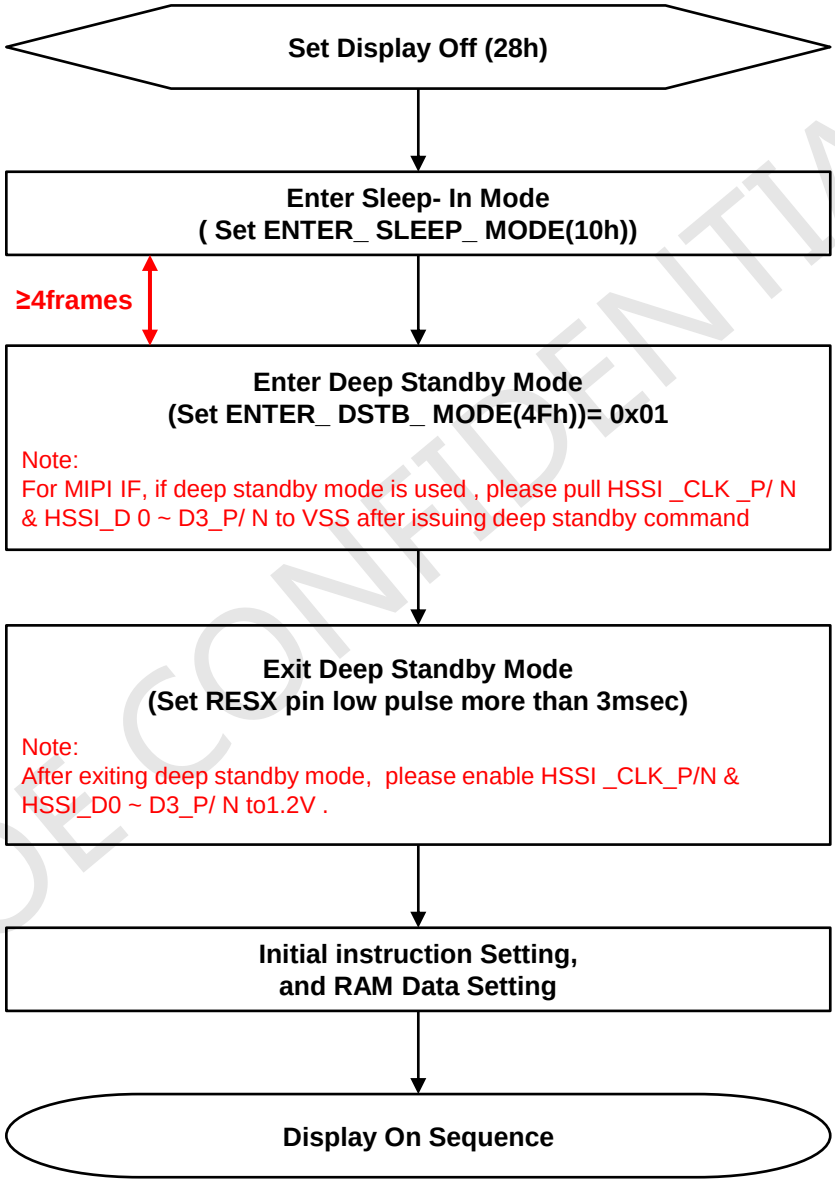
RESX Pulse	*Action*
Shorter than 5μs	*Reset Rejected*

- *During the Resetting period, the display will be blanked(The display is entering blanking sequence, which maximum time is 120 ms, when Reset*
  Starts at Sleep-Out status. The display remains the blank state in Sleep-In mode). Then return to Default condition for Hardware Reset.
- *Spike Rejection also applies during a valid reset pulse as shown below:*



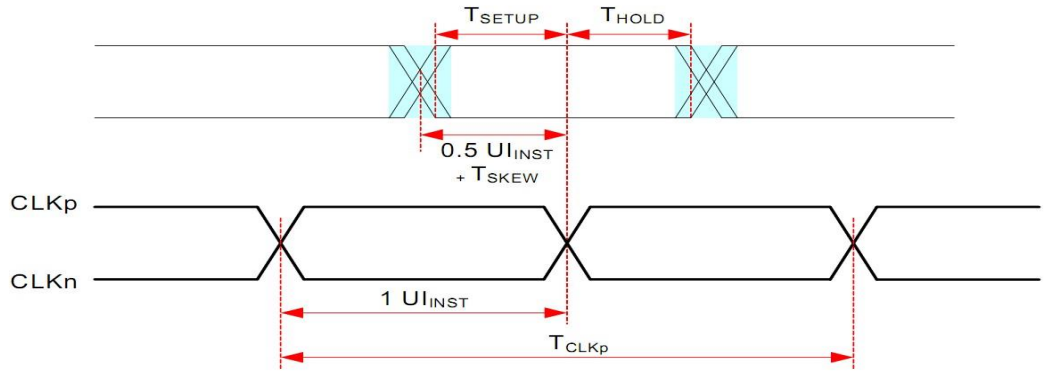
- *When Reset applied during Sleep-In Mode.*
- *When Reset applied during Sleep-Out Mode.*
- *It is necessary to wait 10ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 ms.*

7.3 Deep Standby Mode Timing



7.4 MIPI Interface Characteristics

High Speed Data Transmission: Data-Clock Timing

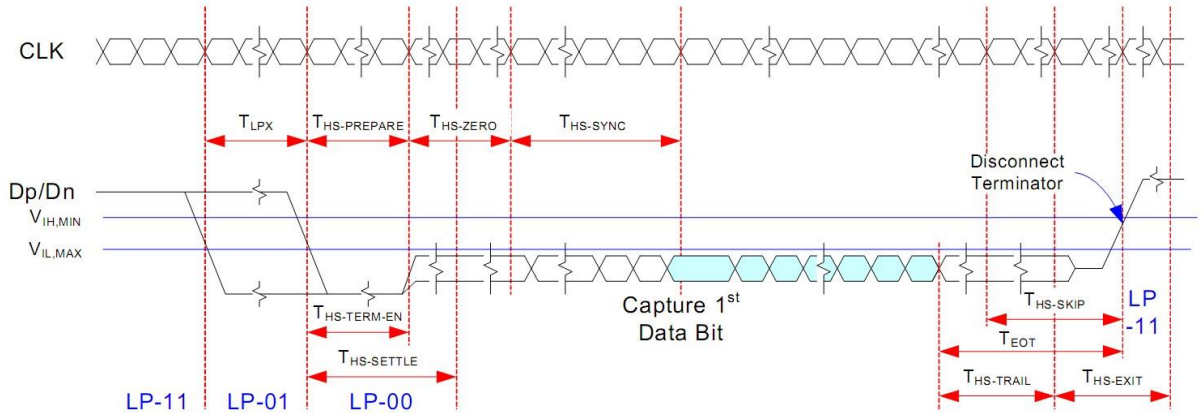


Item	Symbol	Min.	Typ.	Max.	Unit	Notes
UI instantaneous	UI_{INST}	1		4	ns	1,2,7
Data to Clock Skew [measured at tansmitter]	T_{SKEW}[TX]	-0.15		0.15	UI_{INST}	3
Data to Clock Setup Time [measured at receiver]	T_{SETUP}[RX]	0.15		0.15	UI_{INST}	4
Data to Clock Hold Time [measured at reciever]	T_{HOLD}[RX]	0.15		0.15	UI_{INST}	4
20% - 80% rise time and fall time	t_R/ t_F	150			ps	6
				0.3	UI_{INST}	5

Note :

1. *This value corresponds to a minimum 250 Mbps data rate.*
2. *The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.*
3. *Total silicon and package delay budget of 0.3* UIINST when D-PHY is supporting maximum data rate = 1Gbps.*
4. *Total setup and hole window for receiver of 0.3* UIINST when D-PHY is supporting maximum data rate = 1Gbps.*
5. *Applicable when operating at HS bit rates ≤1 Gbps (UI ≥1 ns).*
6. *Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤1 Gbps (UI ≥1 ns), should not use values below 150 ps.*
7. *For MIPI speed limitation:*
   [1] Per lane bandwidth is 1Gbps,
   [2] Total Bit Rate: 4Gbps for 8-8-8; 2.67 Gbps for 6-6-6; and for5-6-5.

High-Speed Data Transmission in Bursts

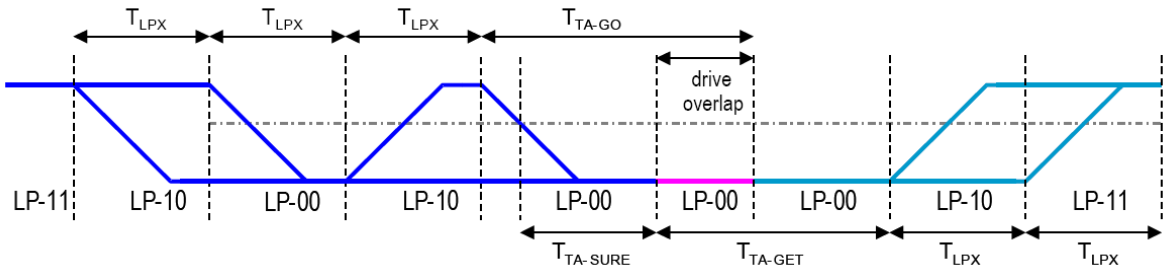


Item	Symbol	Min.	Typ.	Max.	Unit
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of tHS-TRAIL or tCLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12 UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

Note :

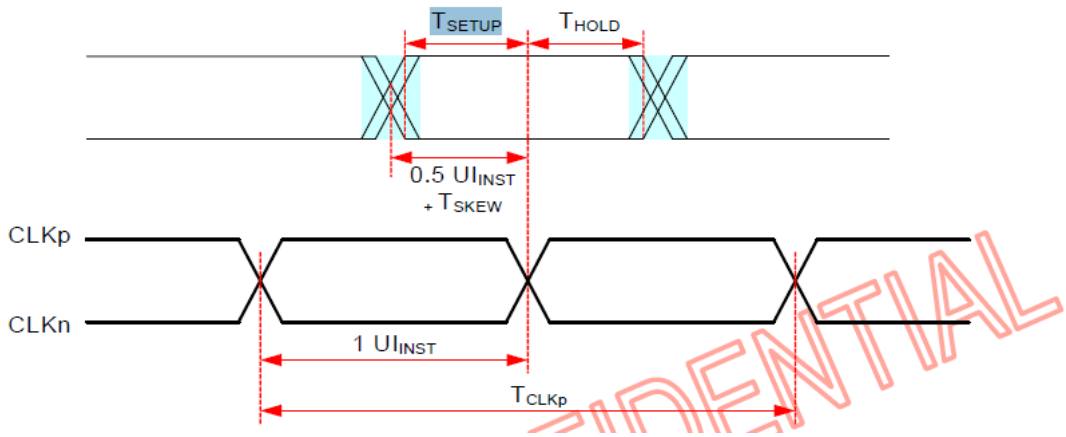
1. *The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.*
2. *UI means Unit Interval, equal to one half HS the clock period on the Clock Lane.*
3. *TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.*

Turnaround Procedure

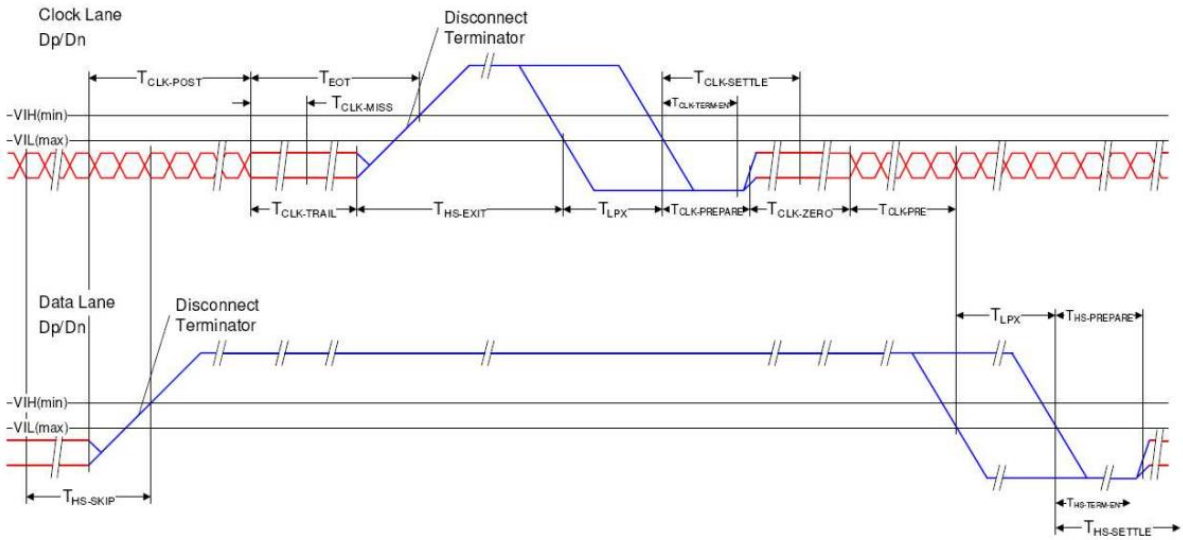


Item	Symbol	Min.	Typ.	Max.	Unit
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	50		75	ns
Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		$2T_{LPX}$	ns
Time to drive LP-00 by new TX	T_{TA-GET}		$5T_{LPX}$		ns
Time to drive LP-00 by new TX	T_{TA-GO}		$4T_{LPX}$		ns

High Speed Data Transmission: Data-Clock Timing



Switching the Clock Lane between Clock Transmission and Low-Power Mode

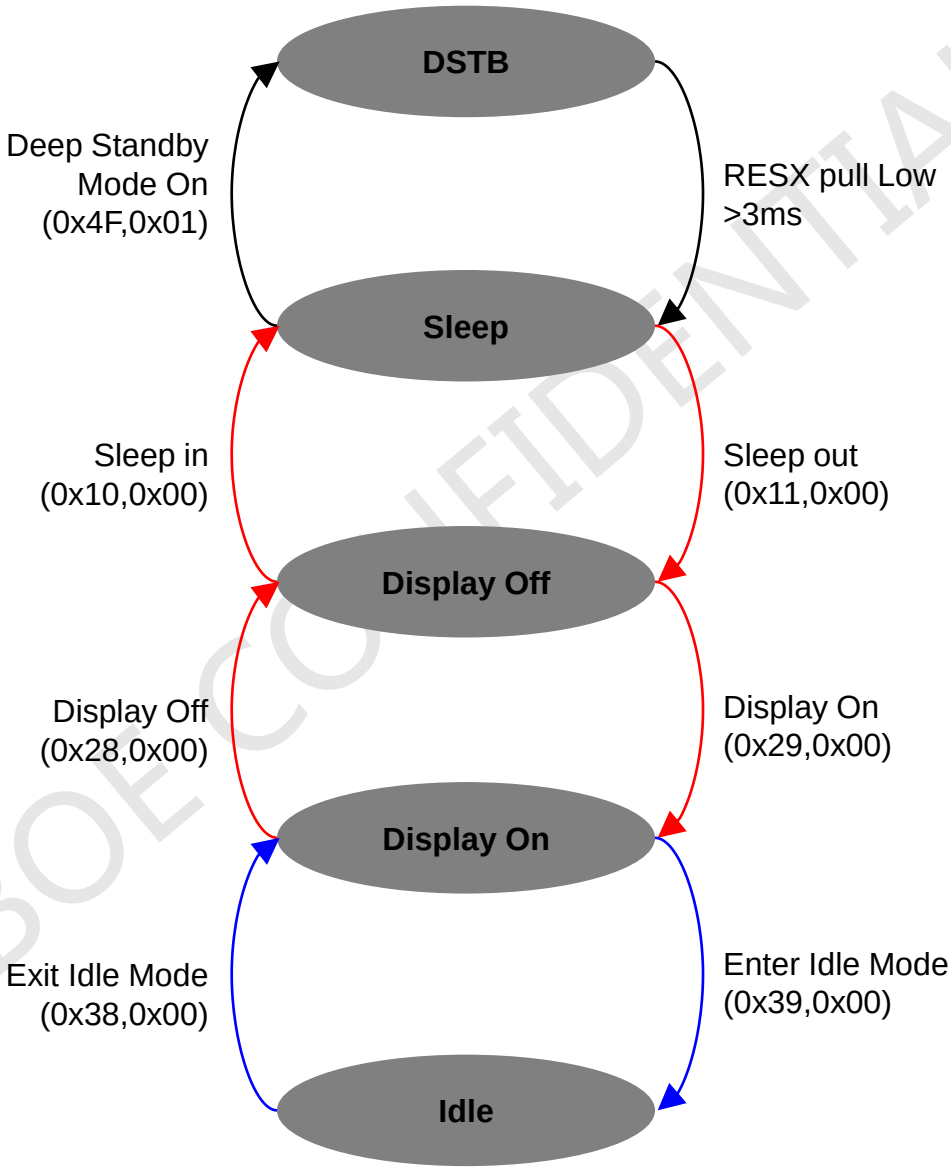


Item	Symbol	Min.	Typ.	Max.	Unit
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60ns+52 UI			ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$			60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38		95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	300			ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8			UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60			ns

Note：

1. *In one Port MIPI, the Tclk-post and Tclk-pre Spec is only define between the CLK lane and Data lanes of each port.*
2. *In Two Port MIPI, the Tclk-post and Tclk-pre Spec is not only define between the DSI2A_CLK lane and DSI2A_Data lanes, but also define between the DSI2B_CLK lane and DSI2A_Data lanes. For DSI21_CLK lane,DSI2B_Data lanes and DSI2A_Data lanes has the same rule.*

7.5 Operating Sequence (for reference only)



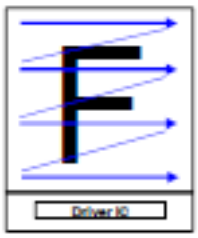
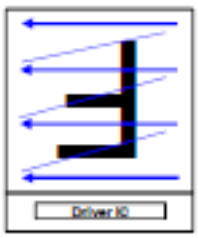
7.6 Initial Code Setting

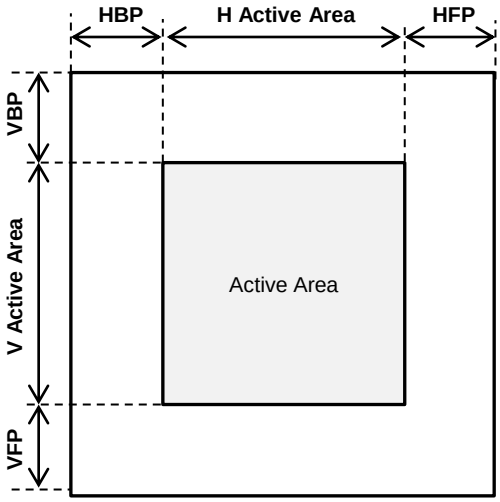
☐ Speed & Porch Setting (for reference only)

Item			Symbol	Min.	Typ.	Max.	Unit
Speed*	Frame Rate		-	-	90		Hz
	Line Time		-	-	3.2	-	us
	Dot CLK		-	-	TBD	-	MHz
	MIPI Speed		-	-	TBD	-	Mbps
Porch	Horizontal	Horizontal total time	Htotal	-	TBD	-	dot
		Horizontal Active time	Hactive	1440			dot
		Horizontal Pulse Width	Hsync	-	-	-	dot
		Horizontal Back Porch	HBP	-	TBD	30	dot
		Horizontal Front Porch	HFP	-	TBD	50	dot
	Vertical	Vertical Total	Vtotal	-	TBD	-	line
		Vertical Active	Vactive	1600			line
		Vertical Pulse Width	Vsync	-	-	-	line
		Vertical Back Porch	VBP	-	TBD	10	line
		Vertical Front Porch	VFP	-	TBD	10	line
Lane				-	4	8	Lane

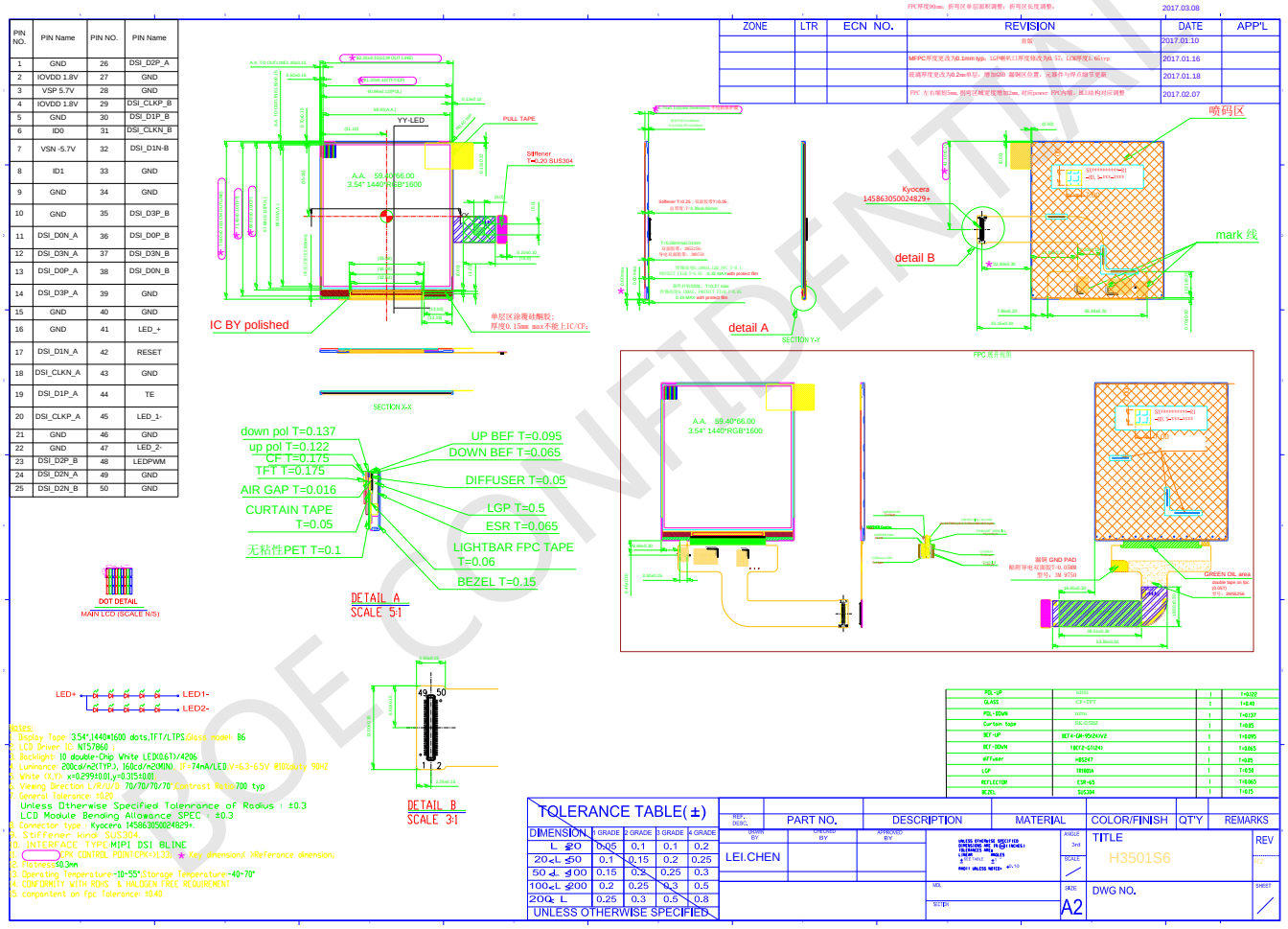
* The Driver IC supports VESA DSC V1.0 and V1.1 Data compression Decoder.

☐ Display Scan Direction

	Data Direction	36h
正向 扫描		00h
反向 扫描		03h



8.0 MECHANICAL CHARACTERISTICS



9.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

<Table 7. Reliability Test Conditions>

No.	Test Items	Conditions
1	High temperature storage	Ta = 70 ℃, 48 hrs
2	Low temperature storage	Ta = -40℃, 48 hrs
3	High temperature & high humidity operation test	Ta = 55 ℃, 90%RH, 48hrs
4	High temperature operation	Ta = 55 ℃, 48 hrs
5	Low temperature operation	Ta = -10 ℃, 48 hrs

Remark：The Reliability test items can only be applied to the BLU 10% on duty Mode

10.0 PACKING INFORMATION

10.1 Packing Description

No.	Description	Quantity	Size (mm)
1	LCM per Box		
2	LCM per Tray		
3	PET Tray		
4	Antistatic Air Bubble Bag		
5	Pulp Molding Pad		
6	Out Box		
7	Belt tape		
8	Distribution label		

Tray 2D Drawing

10.2 Packing Procedure

Step 1	Step 2	Step 3
Step 4	Step 5	Step 6
Step 7	Step8	

10.3 Box Label

T.B.D.

11.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose Power, DSI signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken.
- We recommend to use the original shipping packages.